AD-A038 195 CARNEGIE-MELLON UNIV PITTSBURGH PA DEPT OF COMPUTER --ETC F/G 9/2
CMU-11 ENGINEERING DOCUMENTATION.(U)
JAN 77 S H FULLER, T M MCWILLIAMS F44620-73-C-0074
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CMU-11 ENGINEERING DOCUMENTATION

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Department of Computer Science
Carnegie-Mellon University
Pittsburgh, PA 15213

January 1977

See 1473

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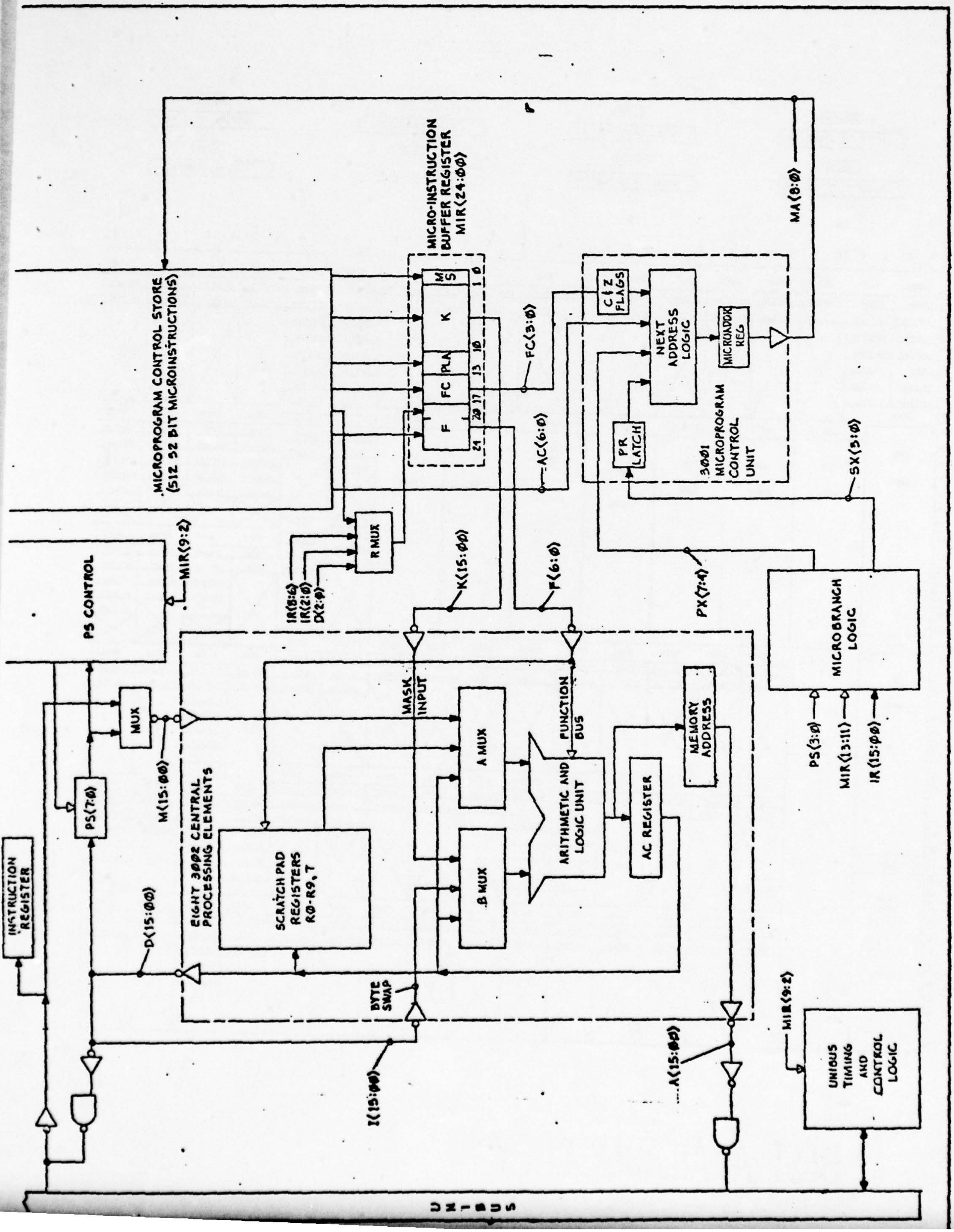
A. D. BLOSE
Technical Information Officer

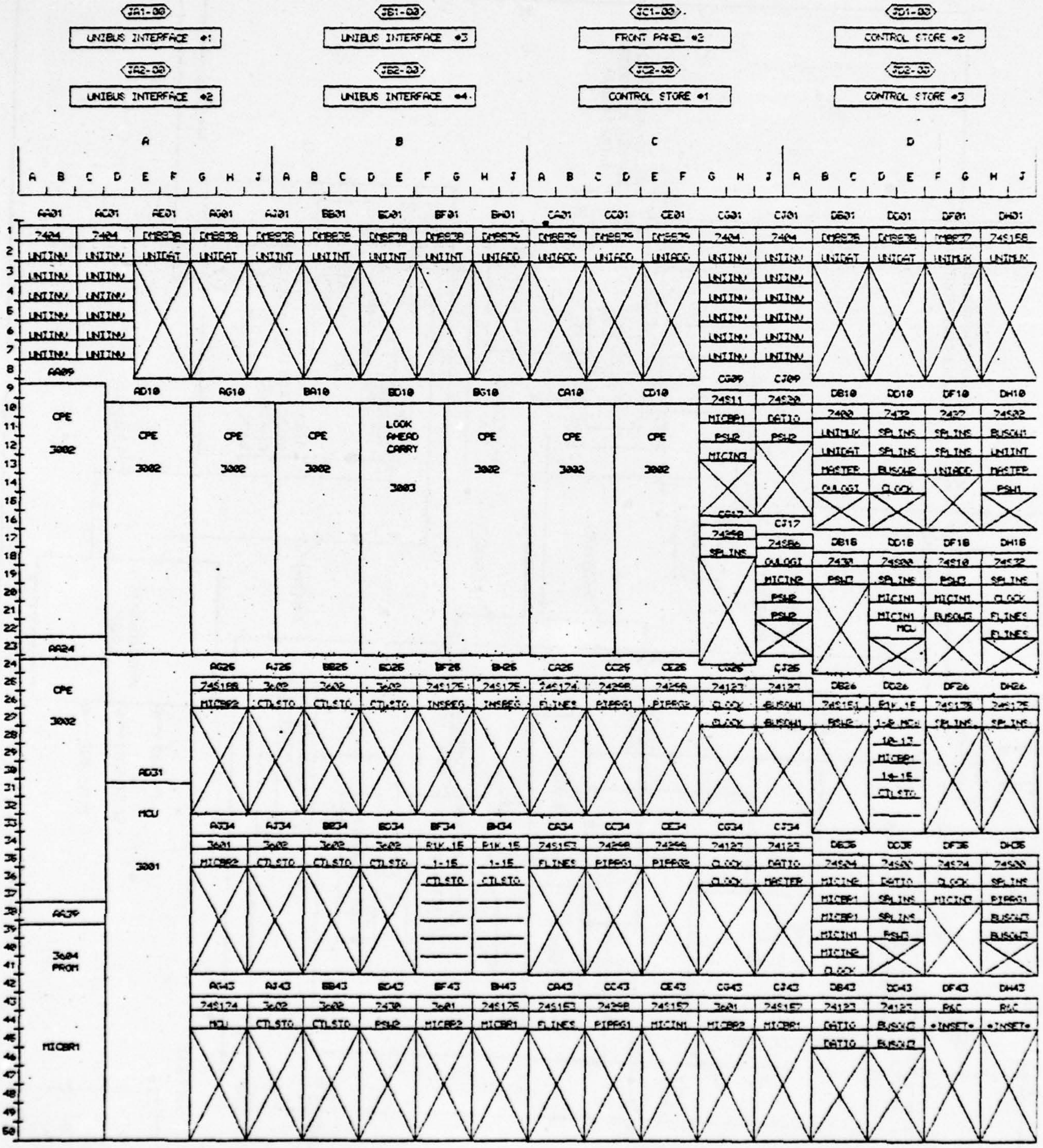
ABSTRACT

The CMU-11 is a microprogrammable processor built with the Intel 3000 microcomputer set that emulates the PDP-11 architecture. In addition, it has been designed to provide full Unibus support. The enclosed documentation gives the details of the CMU-11 design. This documentation has been generated in conjunction with the Stanford Drawing System, the SAGE simulator, and the Intel 3000 microassembler. Those hoping to do any further development of the CMU-11 design are encouraged to also use these design aids and all of the CMU-11 design information shown here (and other information such as ROM contents and wirelists) are available on magnetic tape. See the following report for an introductory discussion and evaluation of the CMU-11:

McWilliams, T. M., S. H. Fuller, and W. H. Sherwood, "Using LSI Processor Bit-Slice to Build a PDP-11: A Case Study in Microcomputer Design," Technical Report, Department of Computer Science, Carnegie-Mellon University, Pittsburgh, PA, January 1976.

CONTENTS


MICROPROGRAM CONTROL STORE
(512 32 BIT MICROINSTRUCTIONS)
MICRO-INSTRUCTION
BUFFER REGISTER
MIR(24:00)
F
FC
PLA
K
M
S
24
20
17
13
10
1
0
MA(8:0)
FC(3:0)
AC(6:0)
C&Z
FLAGS
NEXT
ADDRESS
LOGIC
MICROADDR
REG
PR
LATCH
3001
MICROPROGRAM
CONTROL
UNIT
SX(3:0)
PS CONTROL
MIR(9:2)
R MUX
IR(8:6)
IR(2:0)
D(2:0)
K(15:00)
F(6:0)
PX(7:4)
MICROBRANCH
LOGIC
PS(3:0)
MIR(13:11)
IR(15:00)
INSTRUCTION
REGISTER
PS(7:0)
MUX
M(15:00)
EIGHT 3002 CENTRAL
PROCESSING ELEMENTS
MASK
INPUT
FUNCTION
BUS
A MUX
B MUX
SCRATCH PAD
REGISTERS
R0-R9,T
ARITHMETIC AND
LOGIC UNIT
AC REGISTER
MEMORY
ADDRESS
D(15:00)
BYTE
SWAP
I(15:00)
A(15:00)
MIR(9:2)
UNIBUS
TIMING
AND
CONTROL
LOGIC
UNI-BUS


JA1-00
UNIBUS INTERFACE #1
JA2-00
UNIBUS INTERFACE #2
JB1-00
UNIBUS INTERFACE #3
JB2-00
UNIBUS INTERFACE #4
JC1-00
FRONT PANEL #2
JC2-00
CONTROL STORE #1
JD1-00
CONTROL STORE #2
JD2-00
CONTROL STORE #3
A
B
C
D
A B C D E F G H J
AA01 AC01 AE01 AG01 AJ01 BB01 BD01 BF01 BH01 CA01 CC01 CE01 CG01 CJ01 DB01 DD01 DF01 DH01
7404 7404 DM8838 DM8838 DM8838 DM8838 DM8838 DM8838 DM8839 DM8839 DM8839 DM8839 7404 7404 DM8835 DM8838 DM8837 74S158
UNIINV UNIINV UNIDAT UNIDAT UNIINT UNIINT UNIINT UNIINT UNIADD UNIADD UNIADD UNIADD UNIINV UNIINV UNIDAT UNIDAT UNIMUX UNIMUX
UNIINV
AA09
CPE
3002
AD10 AG10 BA10 BD10 BG10 CA10 CD10
CPE
3002
LOOK
AHEAD
CARRY
3003
CG09 CJ09
74S11 74S30
MICBR1 DATIO
PSW2 PSW2
MICIN3
CG17
74S50
SPLINS
CJ17
74S86
OULOGI
MICIN2
PSW2
PSW2
DB10 DD10 DF10 DH10
7400 7432 7432 74S02
UNIMUX SPLINS SPLINS BUSCH1
UNIDAT SPLINS SPLINS UNIINT
MASTER BUSCH2 UNIADD MASTER
OULOGI CLOCK PSH1
DB18 DD18 DF18 DH18
7430 74S00 74S10 74S32
PSW2 SPLINS PSW2 SPLINS
MICIN1 MICIN1 CLOCK
MICIN1 BUSCH3 FLINES
MCU FLINES
AA24
CPE
3002
AG26 AJ26 BB26 BD26 BF26 BH26 CA26 CC25 CE26 CG26 CJ26
74S188 3602 3602 3602 74S175 74S175 74S174 74298 74298 74123 74123
MICBR2 CTLSTO CTLSTO CTLSTO INSREG INSREG FLINES PIPRG1 PIPRG2 CLOCK BUSCH1
CLOCK BUSCH1
DB26 DD26 DF26 DH26
74S151 R1K.15 74S175 74S175
PSW2 1-8 MCU SPLINS SPLINS
10-13
MICBR1
14-15
CTLSTO
AD31
MCU
3001
AG34 AJ34 BB34 BD34 BF34 BH34 CA34 CC34 CE34 CG34 CJ34
3601 3602 3602 3602 R1K.15 R1K.15 74S153 74298 74298 74123 74123
MICBR2 CTLSTO CTLSTO CTLSTO 1-15 1-15 FLINES PIPRG1 PIPRG2 CLOCK DATIO
CTLSTO CTLSTO CLOCK MASTER
DB35 DD35 DF35 DH35
74S04 74S00 74S74 74S00
MICIN2 DATIO CLOCK SPLINS
MICBR1 SPLINS MICIN2 PIPRG1
MICBR1 SPLINS BUSCH3
MICIN1 PSW2 BUSCH3
MICIN2
CLOCK
AA39
3604
PROM
MICBR1
AG43 AJ43 BB43 BD43 BF43 BH43 CA43 CC43 CE43 CG43 CJ43 DB43 DD43 DF43 DH43
74S174 3602 3602 7430 3601 74S175 74S153 74298 74S157 3601 74S157 74123 74123 R&C R&C
MCU CTLSTO CTLSTO PSW2 MICBR2 MICBR1 FLINES PIPRG1 MICIN1 MICBR2 MICBR1 DATIO BUSCH3 •INSET• •INSET•
DATIO BUSCH3
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50

JE1-00

JF1-00

FRONT PANEL #1

JE2-00

JF2-00

E									F								
A	B	C	D	E	F	G	H	J	A	B	C	D	E	F	G	H	J

EA01	EC01	EE01	EG01	EJ01	FB01	FD01	FF01	FH01
74S158	74S157	7432	74S151	74S175	74S175	74148	74S74	7404
UNIMUX	PSH3	PSH3	OULOGI	INSREG	INSREG	MICIN1	OULOGI	MASTER
		OULOGI					OULOGI	MASTER
		PSH1						CLOCK
		~~[illegible]~~						PSH1
								PSH2
								PSH2

EA10	EC10	EE10	EG10	EJ10	FB10	FD10	FF10	FH10
7410	74S04	74S02	74S20	74S72	74S00	74S74	74S74	74S74
~~[illegible]~~	SPLINS	MICRP1	OULOGI	MICIN2	MICIN3	BUSOH2	BUSOH2	MICIN3
DATIO	BUSOH3	MICRP1	DATIO	MICIN2	MICIN3	BUSOH2	DATIO	MICIN3
MASTER	DATIO	MICRP1	PSH1	CLOCK	MICIN2			
	SPLINS	MICRP1	OULOGI	PIPRG1	MICIN2			
	CLOCK							
	CLOCK							

EA18	EC18	EE18	EG18	EJ18	FB18	FD18	FF18	FH18
74S11	7420	74S74	7427	74S260	7474	74S03	74S74	74S00
SPLINS	PSH3	BUSOH3	MICIN2	PSH2	PSH3	MICRP1	MICIN2	SPLINS
BUSOH2		DATIO	PSH2	PSH2	PIPRG2	SPLINS	MASTER	SPLINS
BUSOH2			BUSOH2			SPLINS		SPLINS
						UNIINT		SPLINS

EA26	EC26	EE26	EG26	EJ26	FB26	FD26	FF26	FH26
74S175	74148	74S175	[illegible] 15	74S157	74S74	74S175	74S64	74S00
MICRP2	BUSOH2	BUSOH2	1-4	PSH2	MASTER	MICIN2	MICIN2	OULOGI
		BUSOH2	CTLSTO		CLOCK			[illegible]
			7					
			UNIINT					
			MICRP1					
			5,6,8-15					
			SPLINS					

EA35	EC35	EE35	EG35	EJ35	FB35	FD35	FF35	FH35
74S20	7432	74S05	74S08	74S74	74S08	7404	74S04	7402
MCU	MCU	BUSOH2	~~BUSOH1~~	BUSOH1	BUSOH1	UNIINV	UNIINV	OULOGI
MASTER	BUSOH1	DATIO	BUSOH2	DATIO	BUSOH3	UNIINV	UNIINV	OULOGI
	MICRP1	MICIN1	CLOCK	DATIO	INSREG	UNIINV	UNIINV	OULOGI
		MICRP1	OULOGI		DATIO	UNIINV	UNIINV	MICIN1
						UNIINV	UNIINV	
						UNIINV	MICIN2	

EA43	EC43	EE43	EG43	EJ43	FB43	FD43	FF43	FH43
74123	74123	3602	3602	74S175	74175	74259	74S174	74S157
MICIN1	MICIN3	MICRP1	MICRP1	BUSOH2	PSH1	PSH1	PSH1	MICIN1
MICIN2	PIPRG2							

DF43

INSET		
RCD 1,2	MICIN3	3.3U, 15K
RCD 4,5	MICIN3	3.3U, 8.2K
RC 7,10	MICIN3	680P, 12K
R 9	MASTER	10K
R 11	PIPRG2	10K
R 12	BUSOH3	10K
R 14	BUSOH1	5.1K
POT 15	BUSOH1	20K POT
• 3,6	DATIO	POWER

74123
RC NETWORKS

DH43

INSET		
RCD 1,2	DATIO	.005U, 20K
RCD 4,5	BUSOH3	.002U, 20K
RCD 7,8	CLOCK	3.3U, 12K
POT 9	CLOCK	20K POT
R 11	CLOCK	10K
R 12	CLOCK	5.1K
R 14	DATIO	20K
POT 15	DATIO	20K POT
• 3,6	DATIO	POWER

74123
RC NETWORKS

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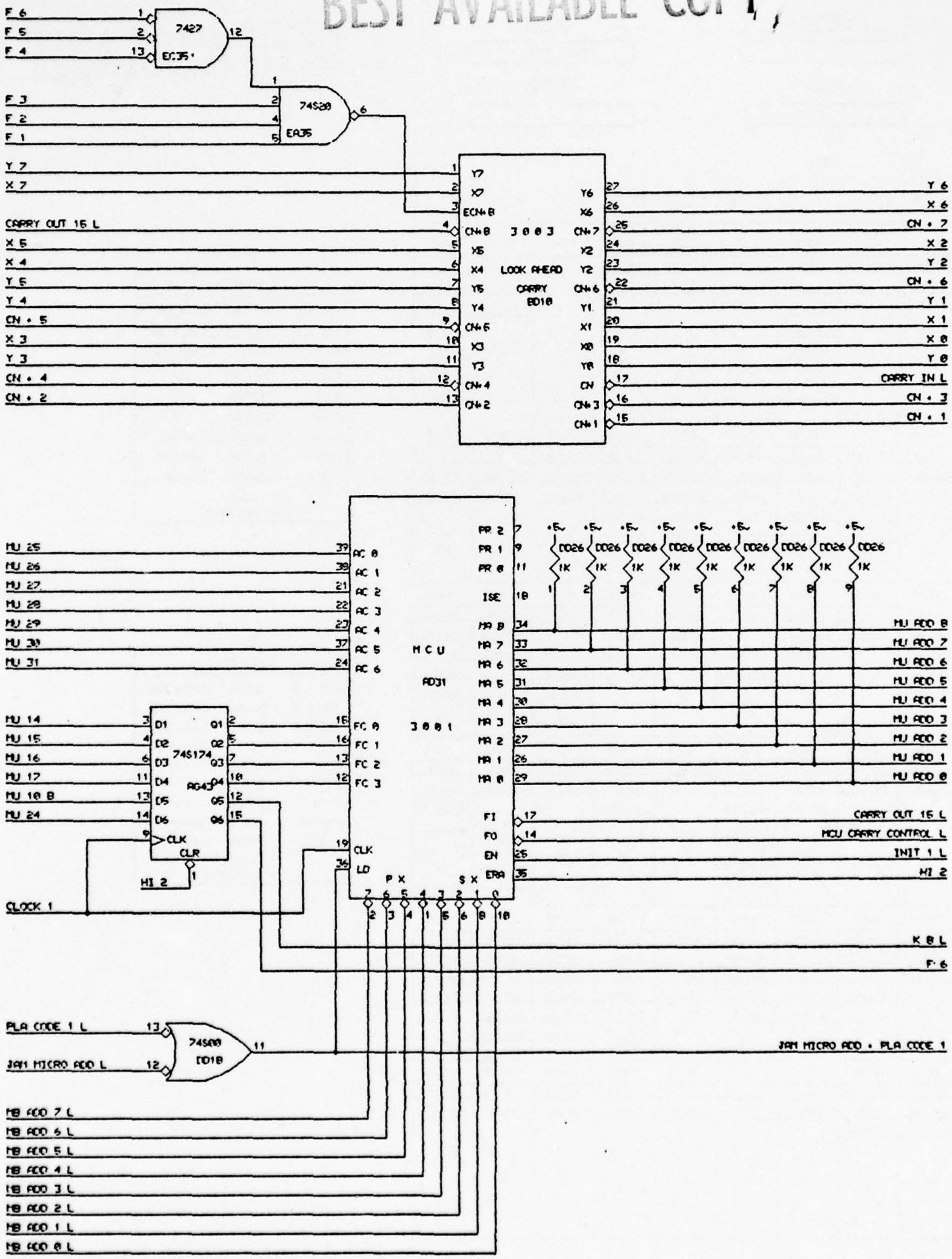

COMPUTER SCIENCE ENGINEERING LAB

TITLE: MICROPROGRAM CONTROL UNIT AND CARRY LOOK-AHEAD

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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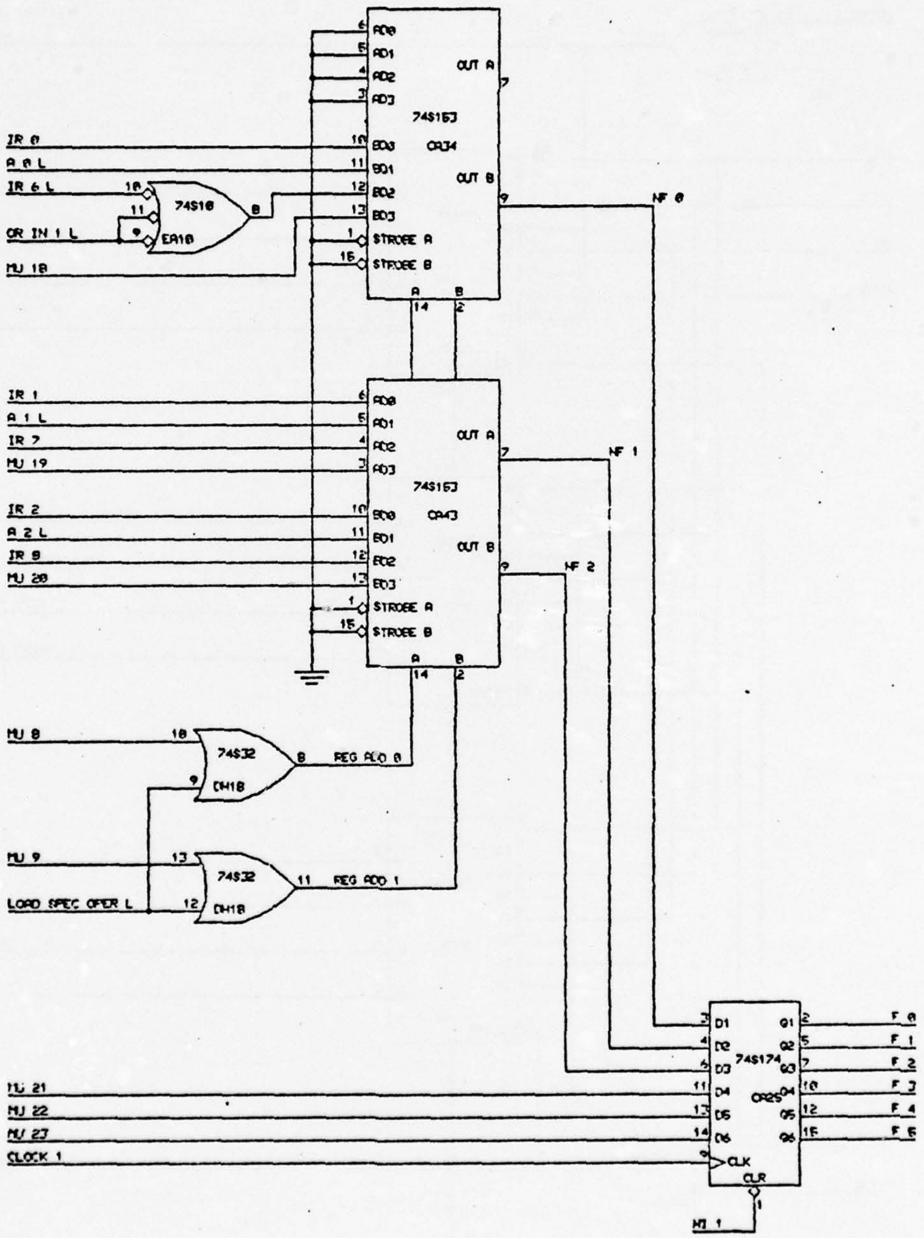

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TITLE: CPE FUNCTION CONTROL LINES

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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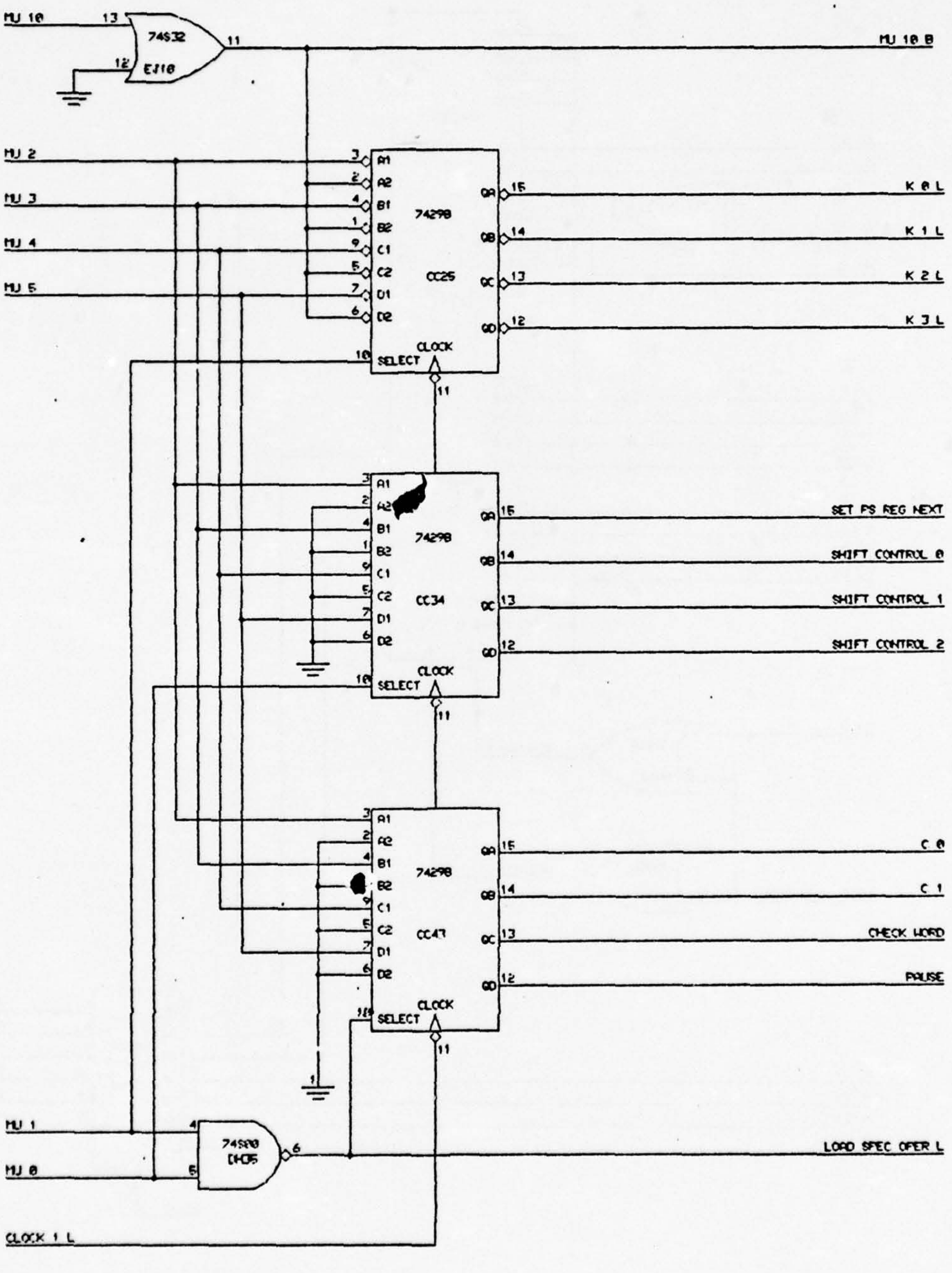

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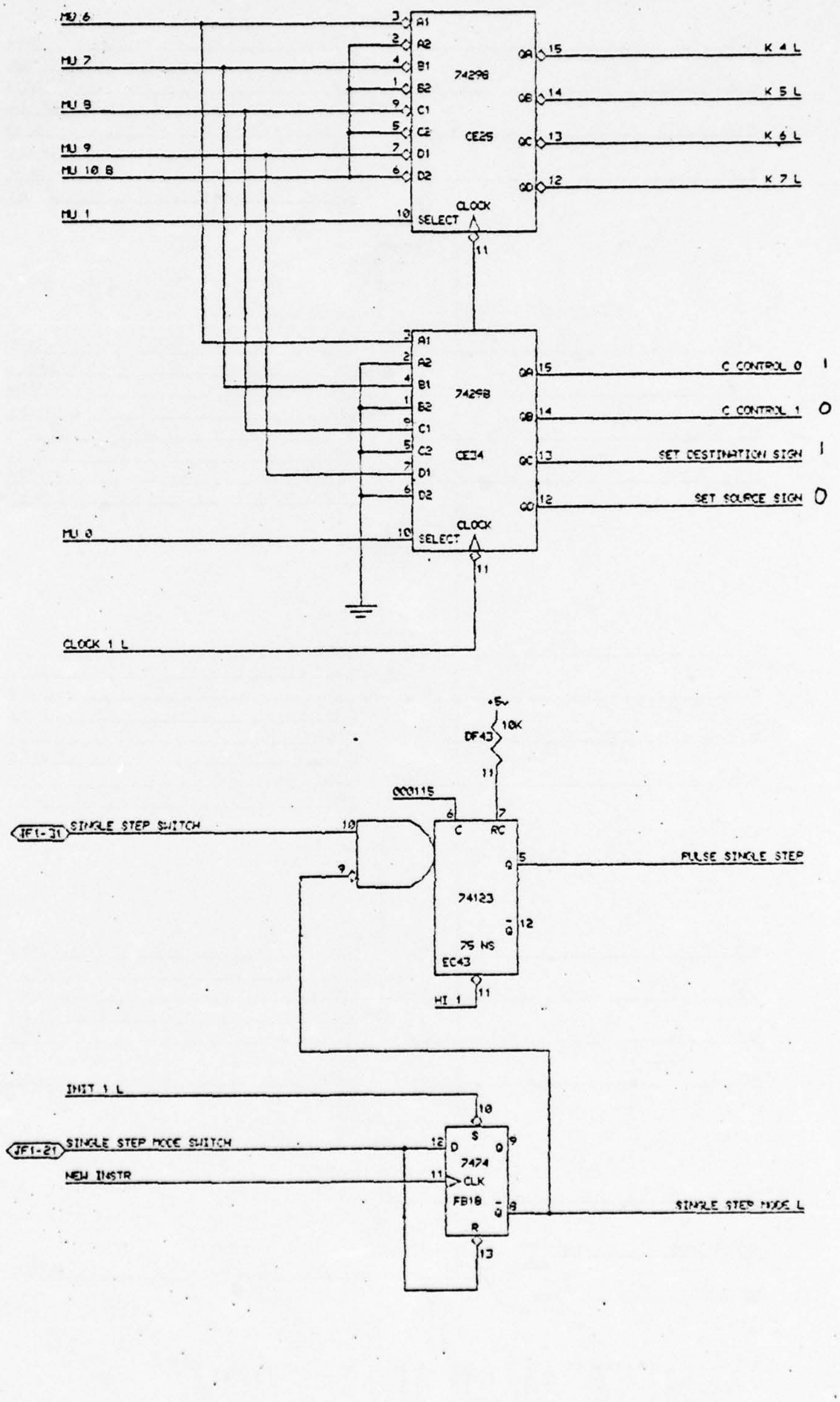

COMPUTER SCIENCE ENGINEERING LAB

TITLE: PIPELINE REGISTER (PART 2)

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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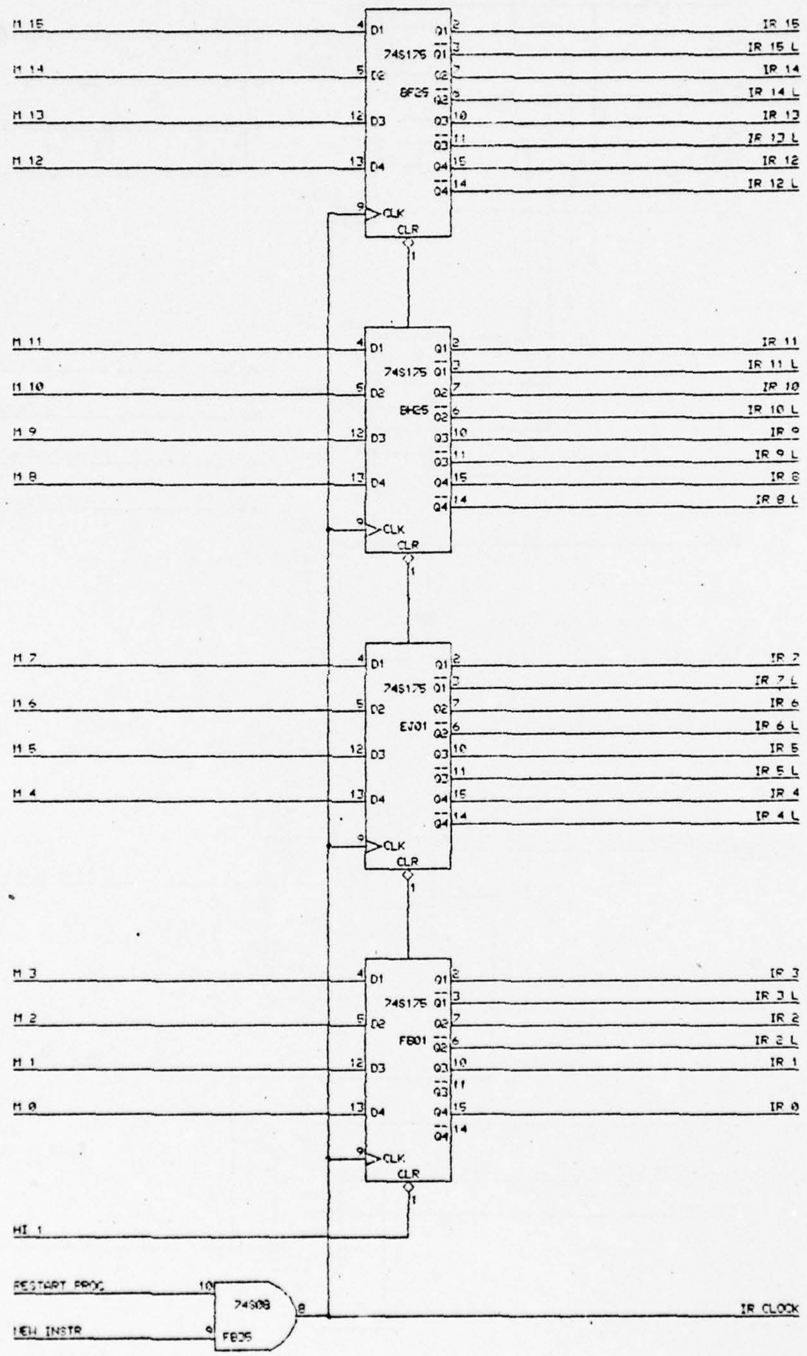

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TITLE: 11 INSTRUCTION REGISTER

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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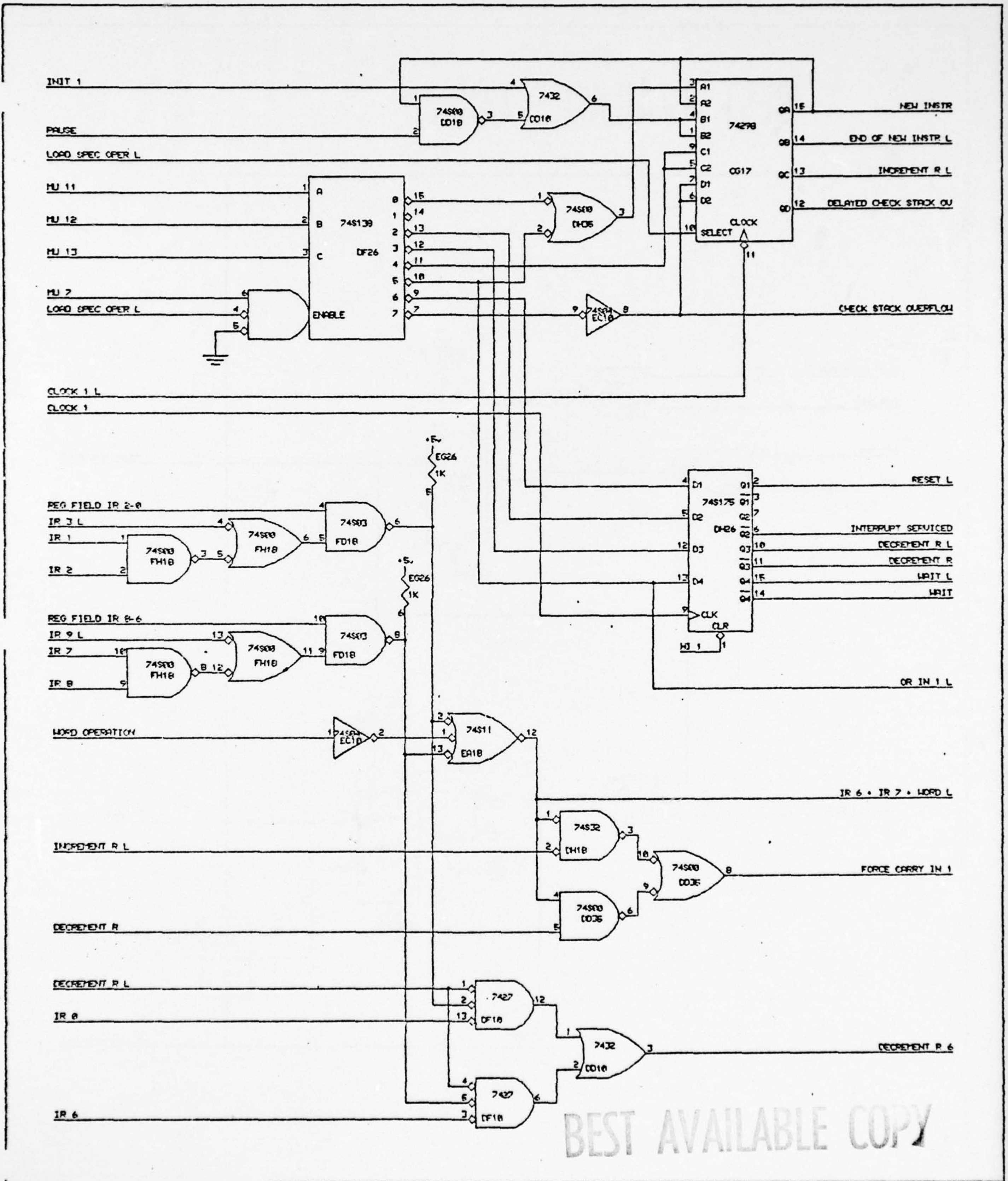

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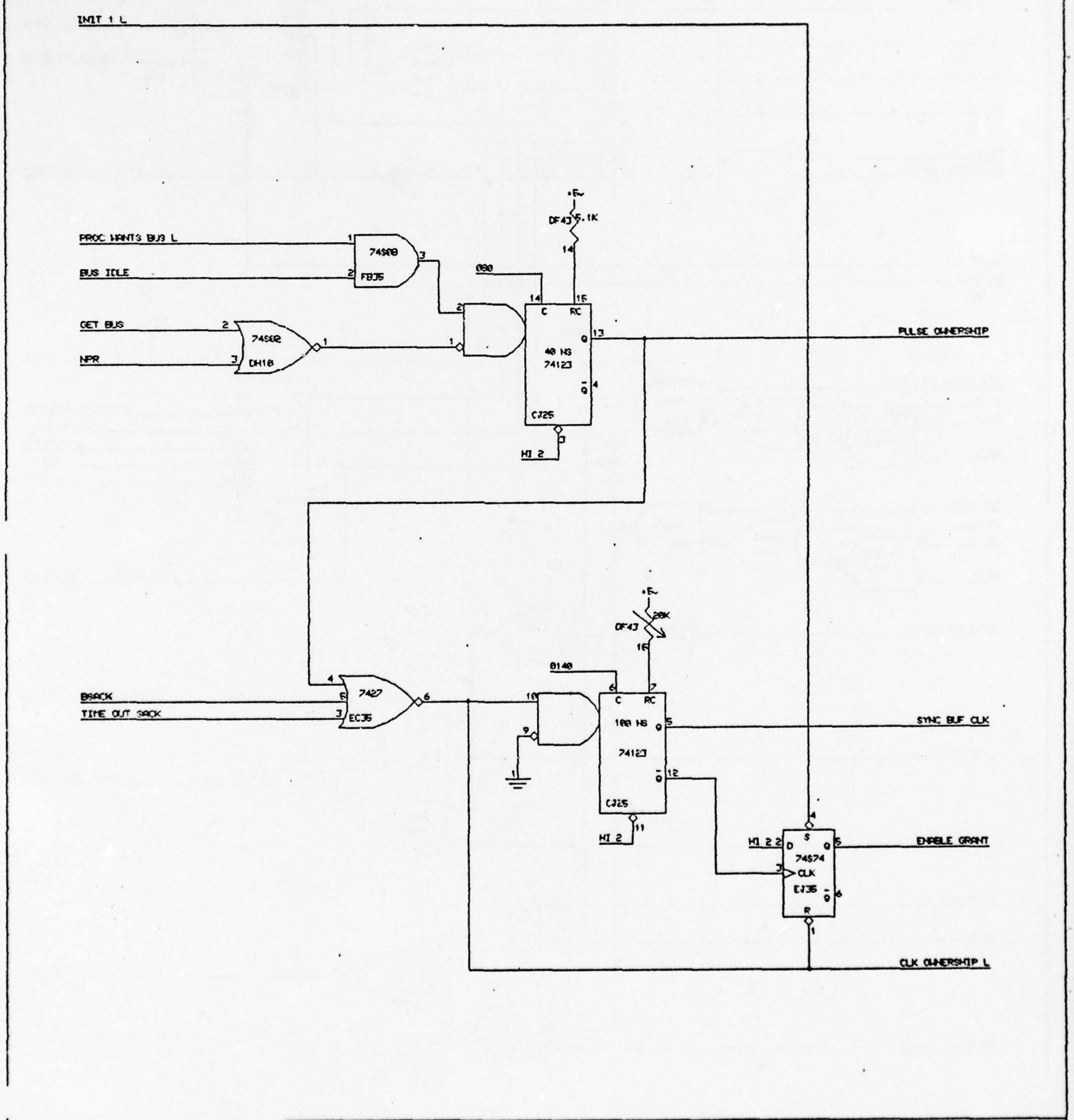

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TITLE: BUS OWNERSHIP

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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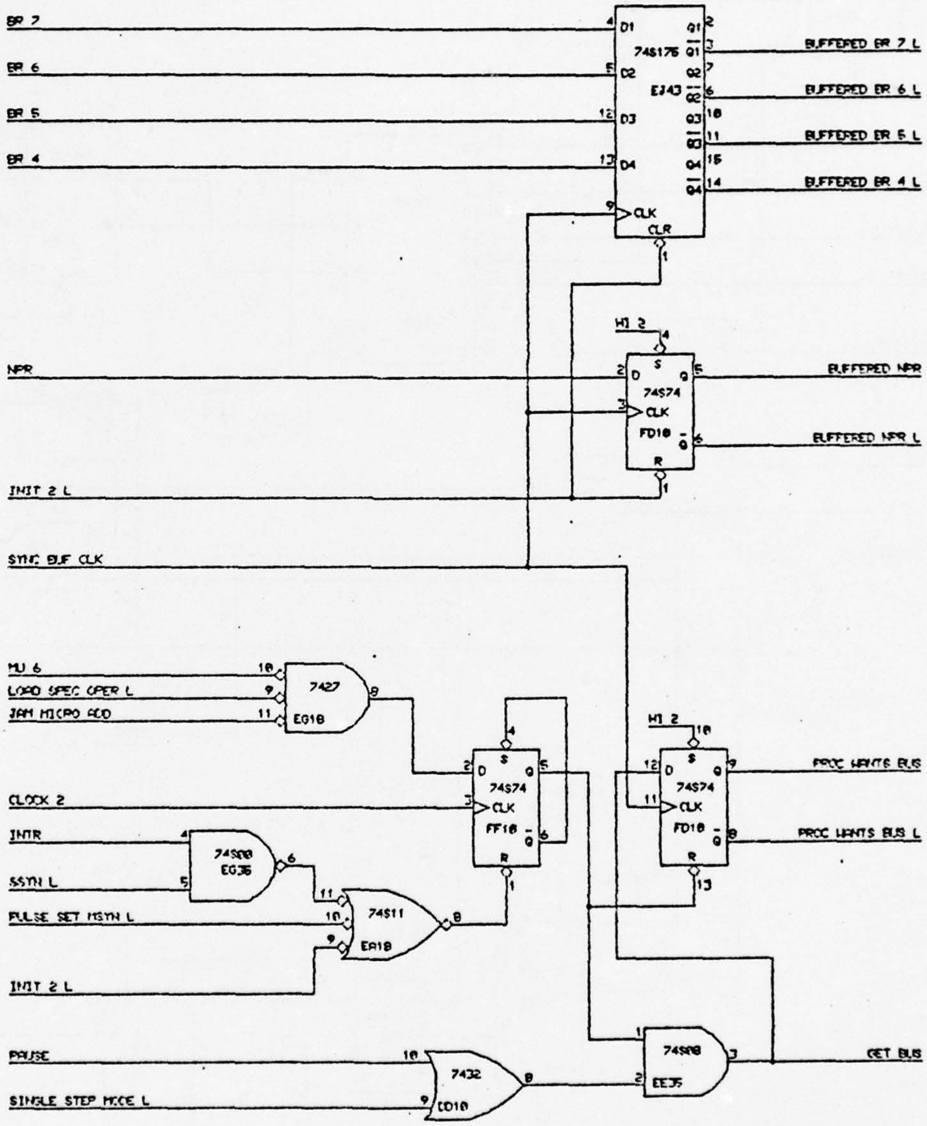

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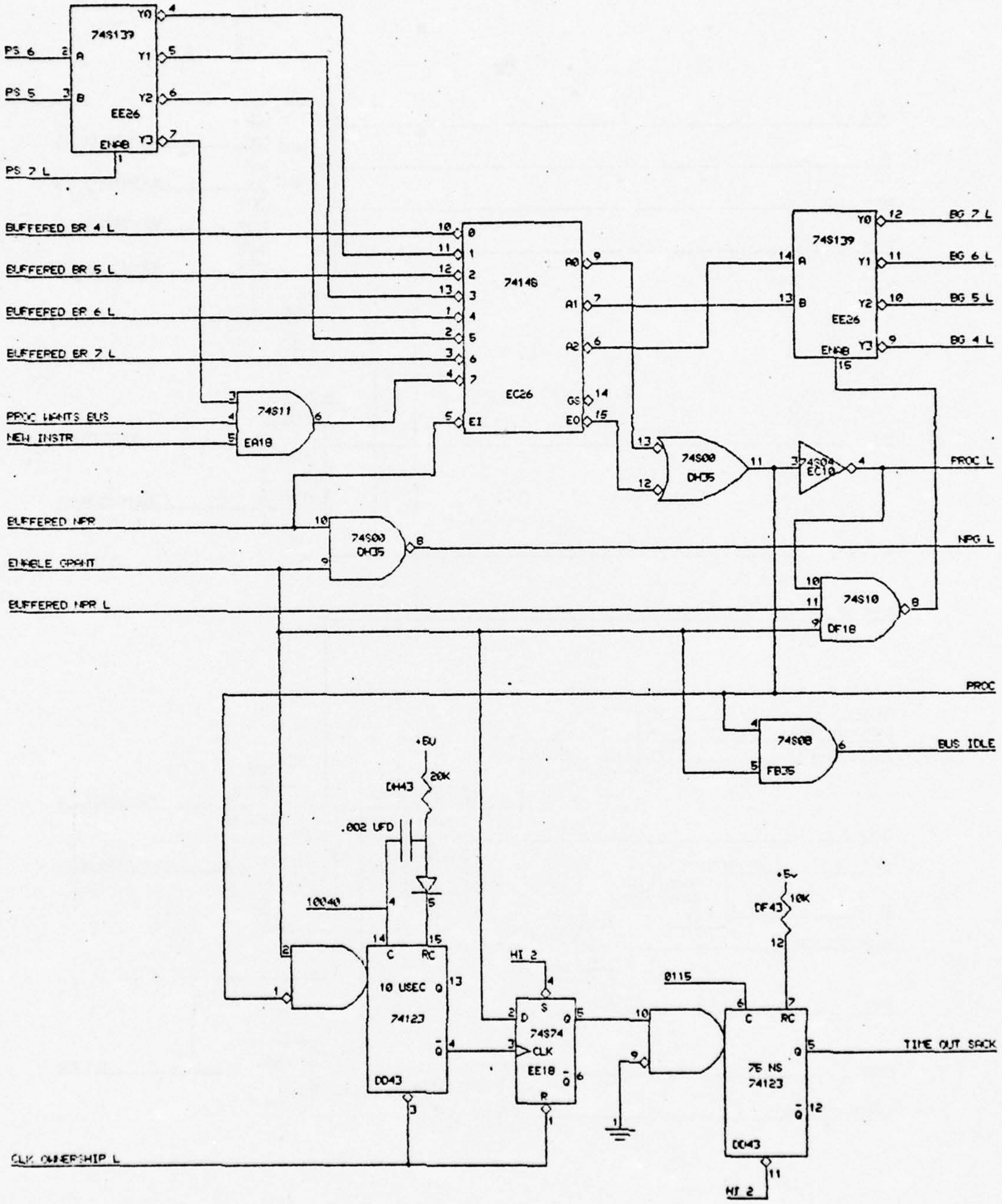

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TITLE: BUS GRANT

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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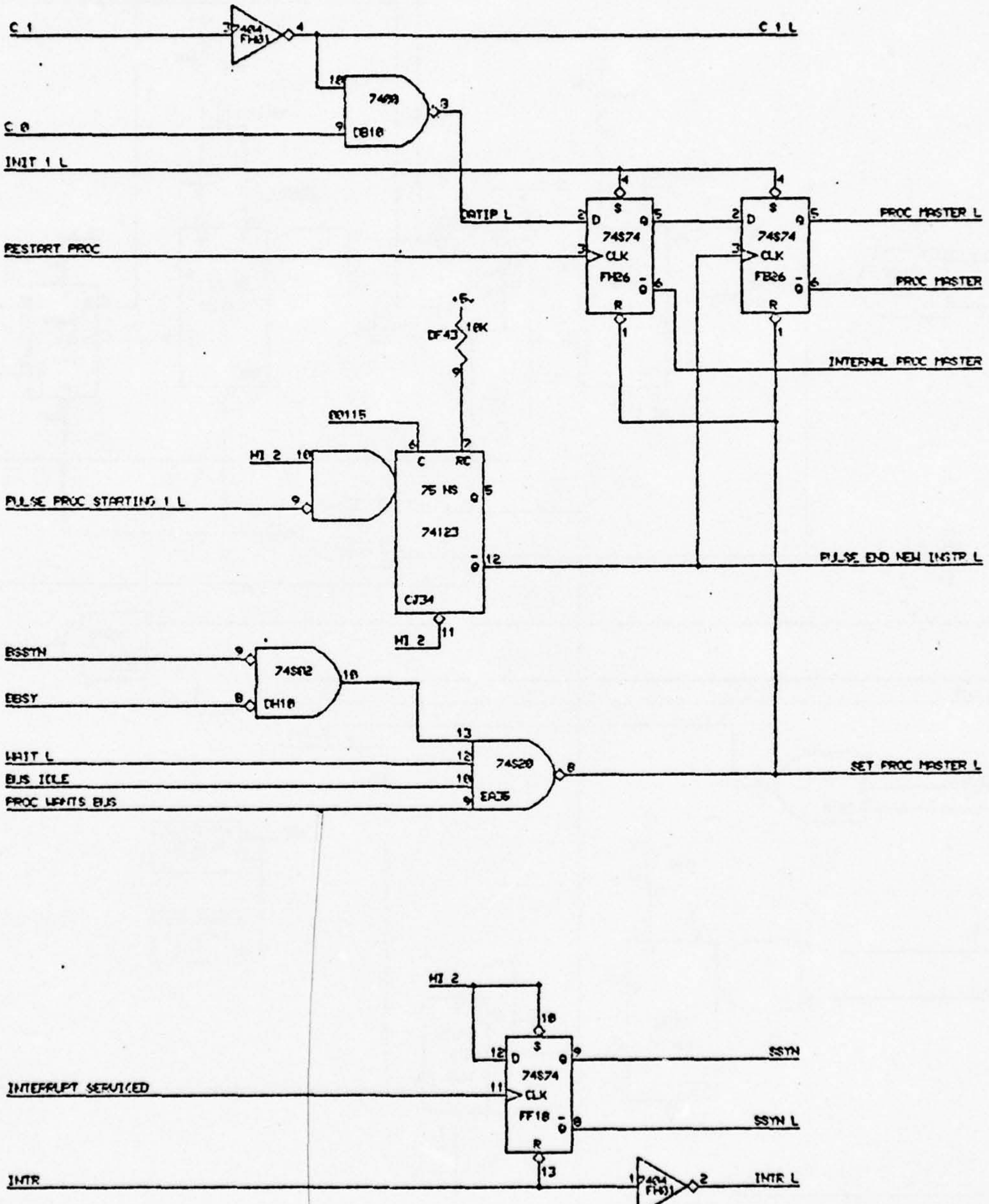

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TITLE:	PROCESSOR MASTER CONTROL
PROJECT:	PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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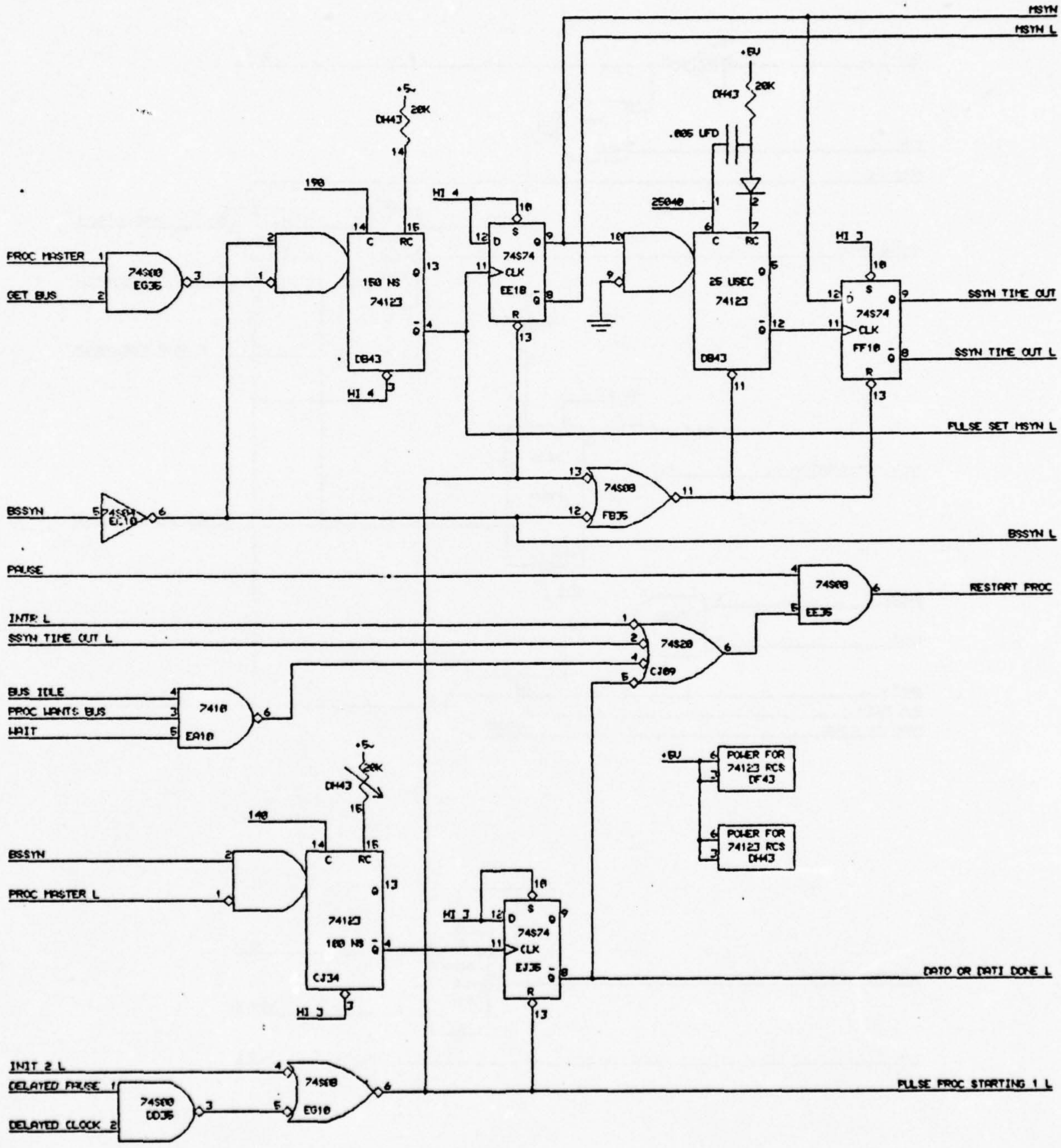

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TITLE: DATI AND DATO LOGIC (PART 1)

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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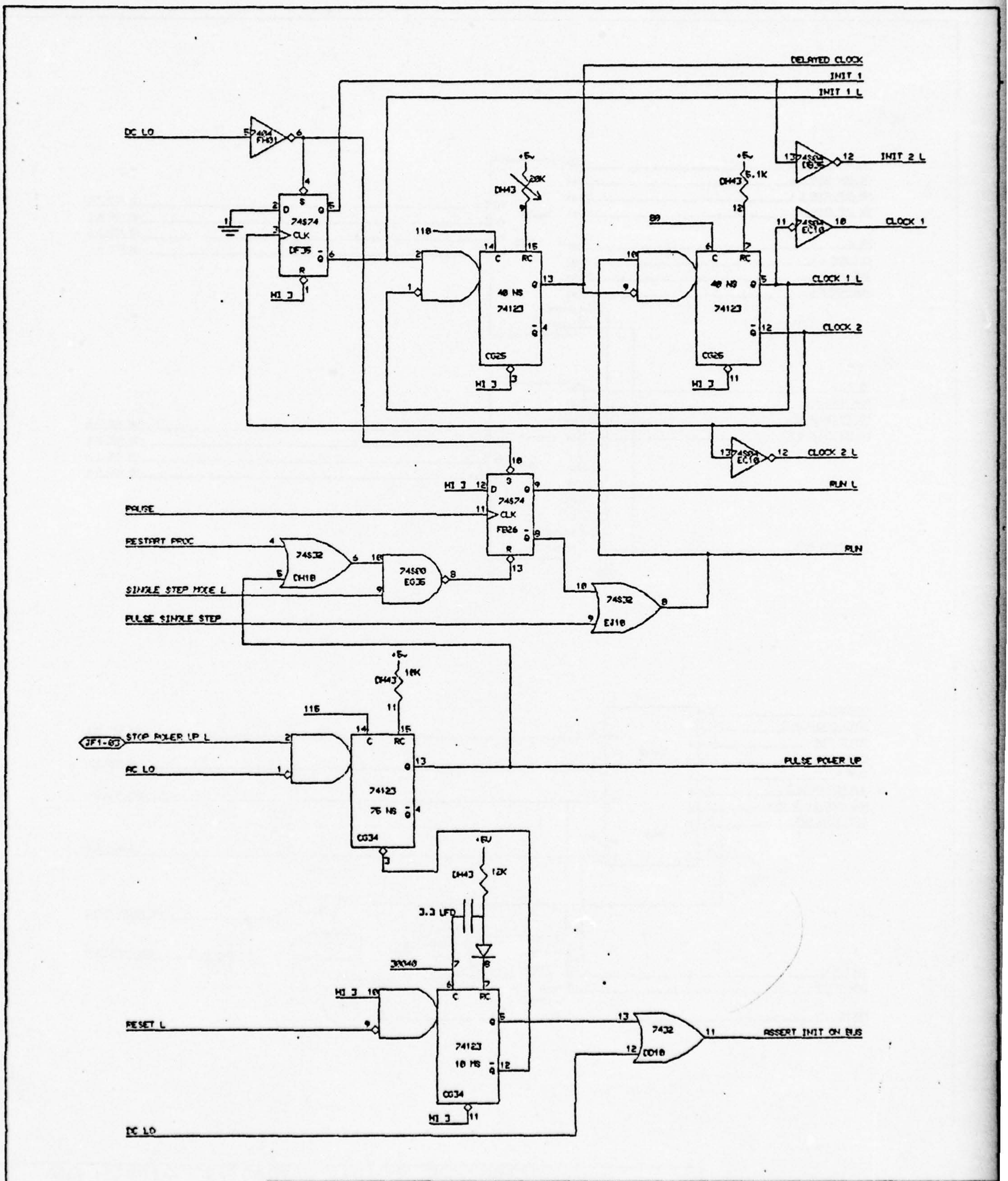

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TITLE: PROCESSOR CLOCK AND INITIALIZATION

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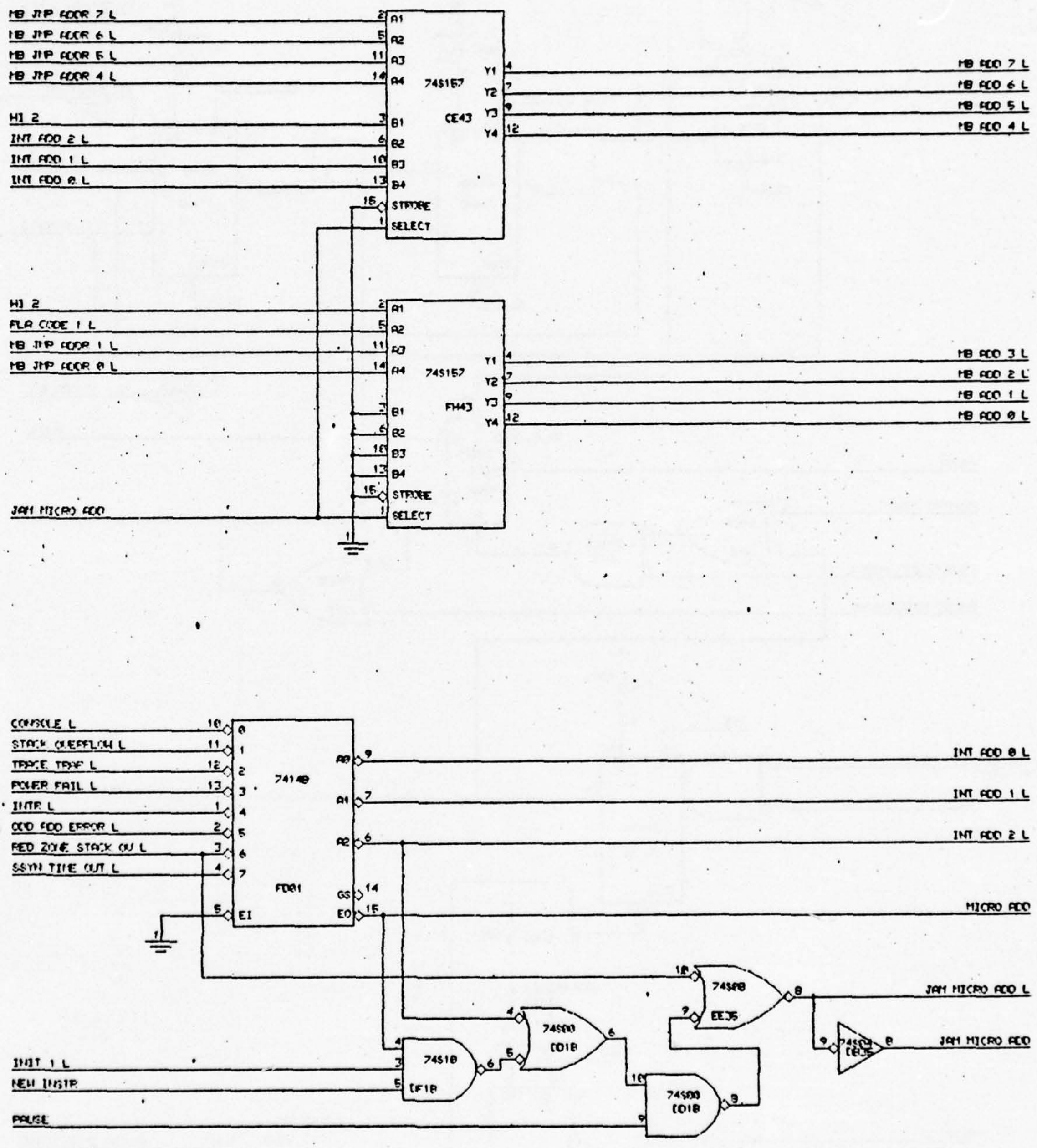

COMPUTER SCIENCE ENGINEERING LAB

TITLE: MICROBRANCH ADDRESS LINES

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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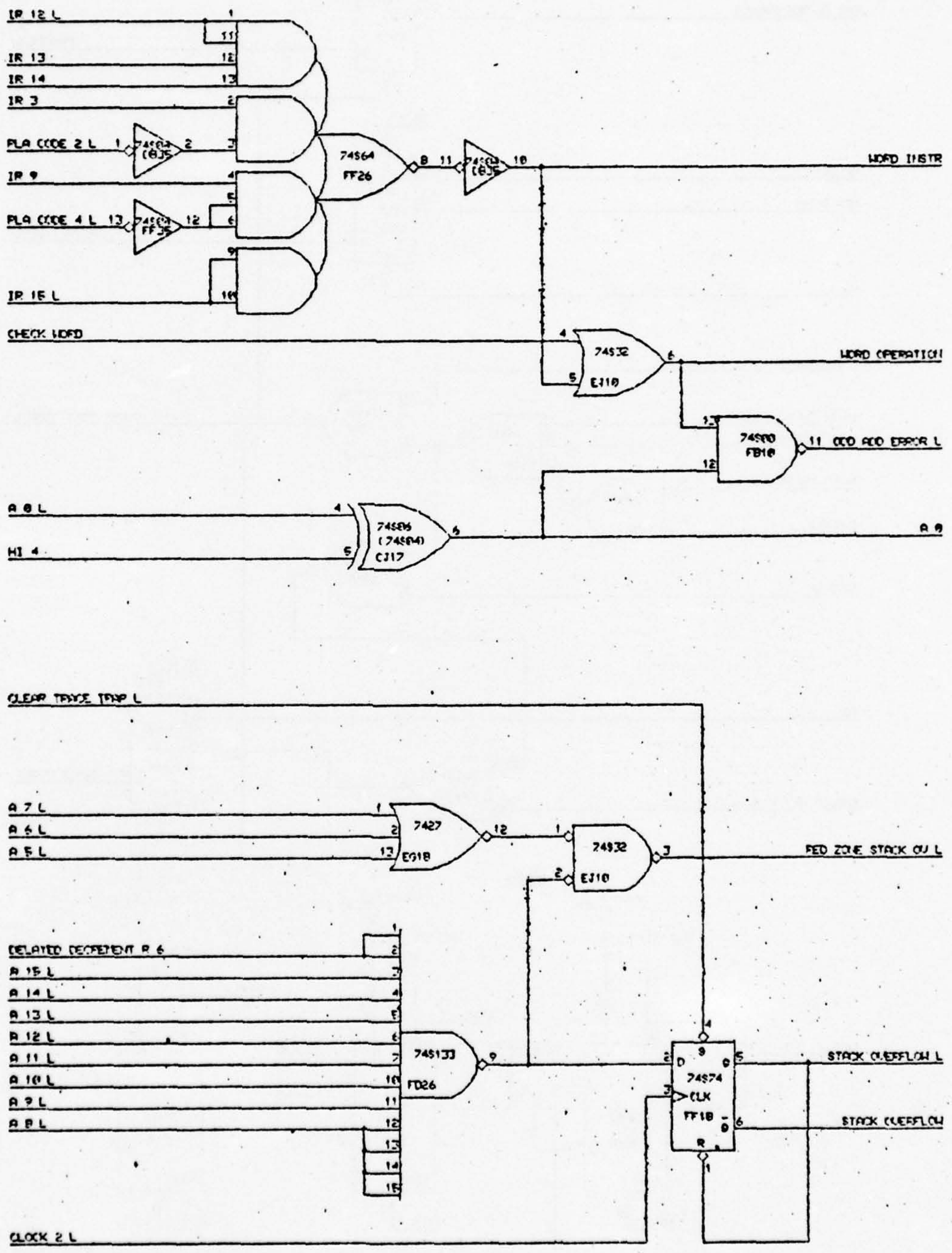

COMPUTER SCIENCE ENGINEERING LAB

TITLE: STACK UNDERFLOW AND ODD ADDR ERRORS

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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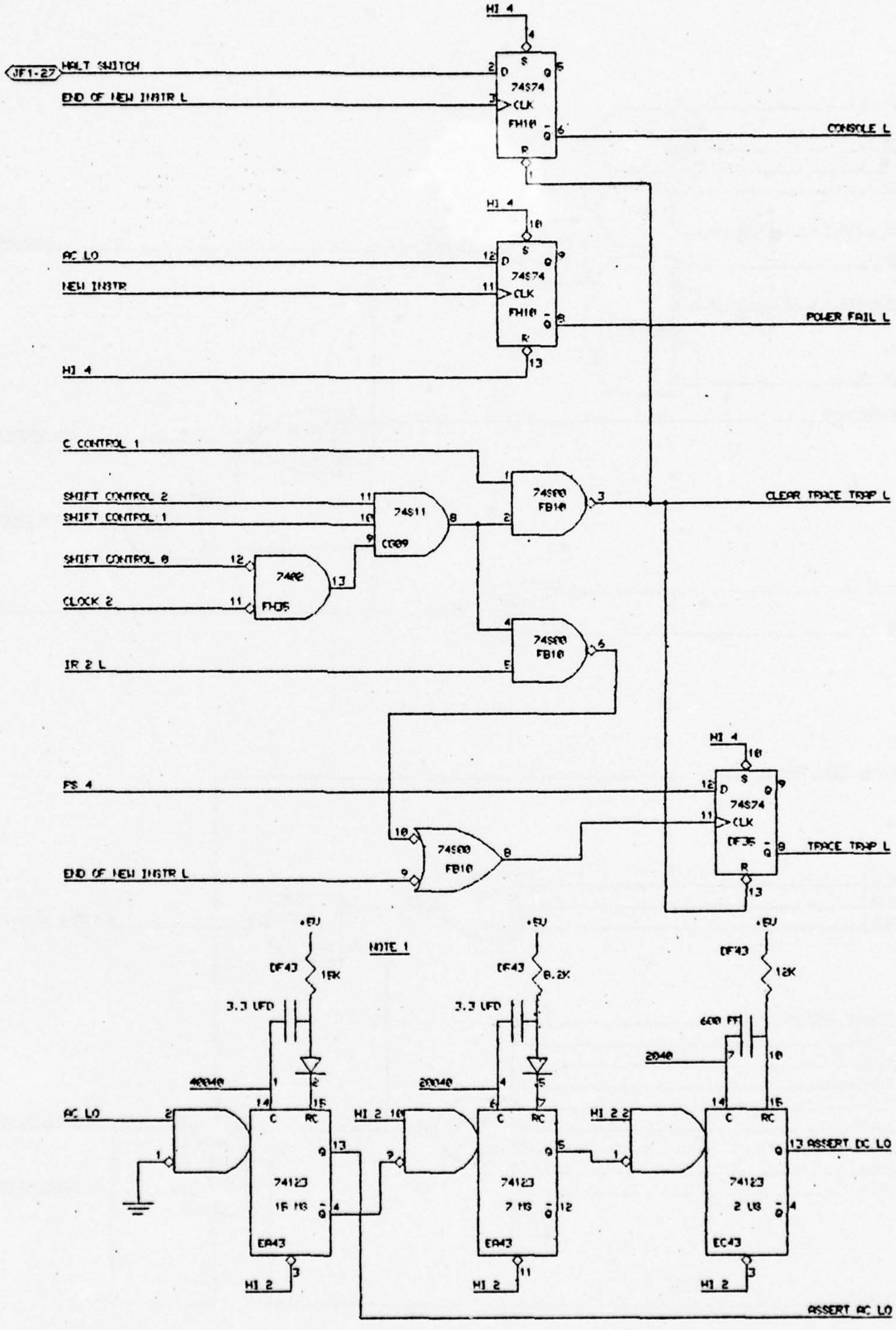

NOTE 1 THIS LOGIC IS TO AVOID EFFECTS OF MULTIPLE AC POWER GLITCHES

COMPUTER SCIENCE ENGINEERING LAB

TITLE: HALT, CONSOLE, AND TRACE TRAPS		
PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR		
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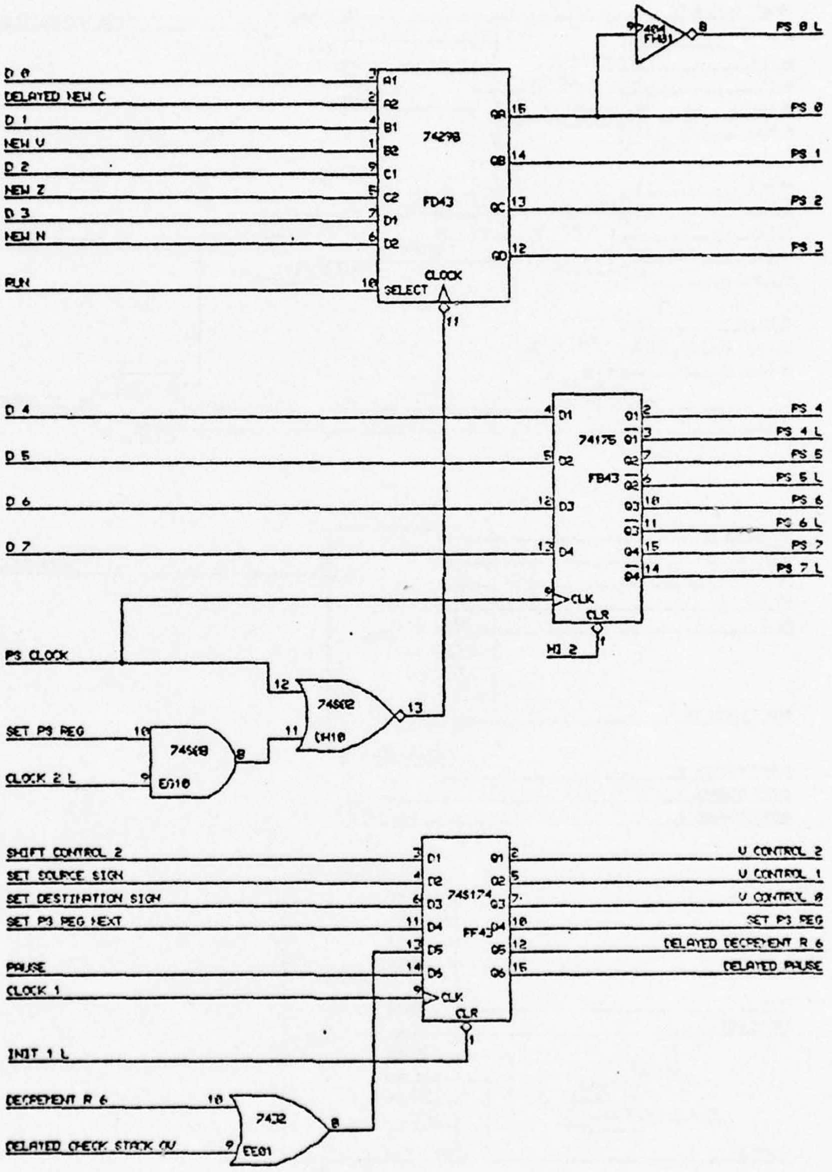

COMPUTER SCIENCE ENGINEERING LAB

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PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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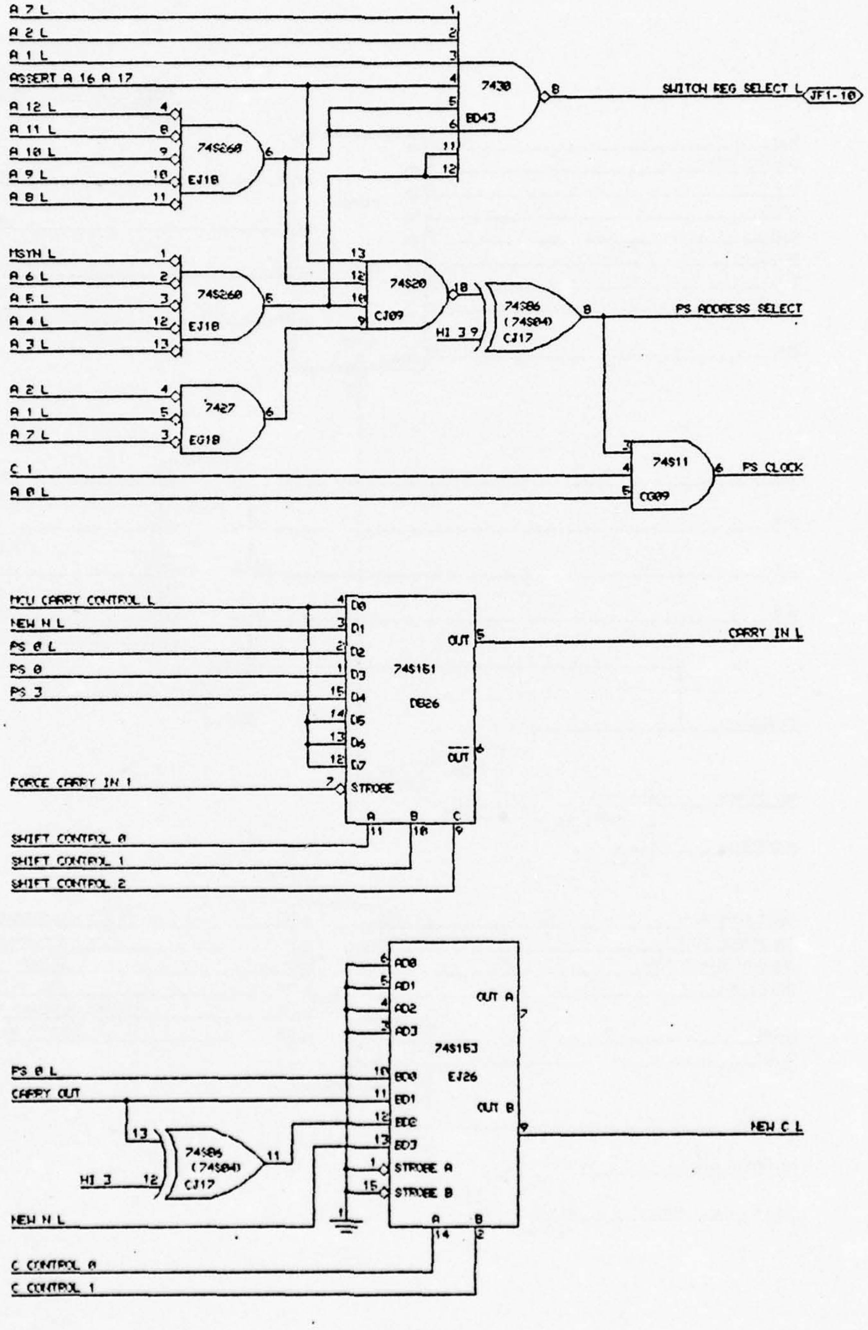

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TITLE: PS ADDRESS AND CARRY IN CONTROL.		
PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR		
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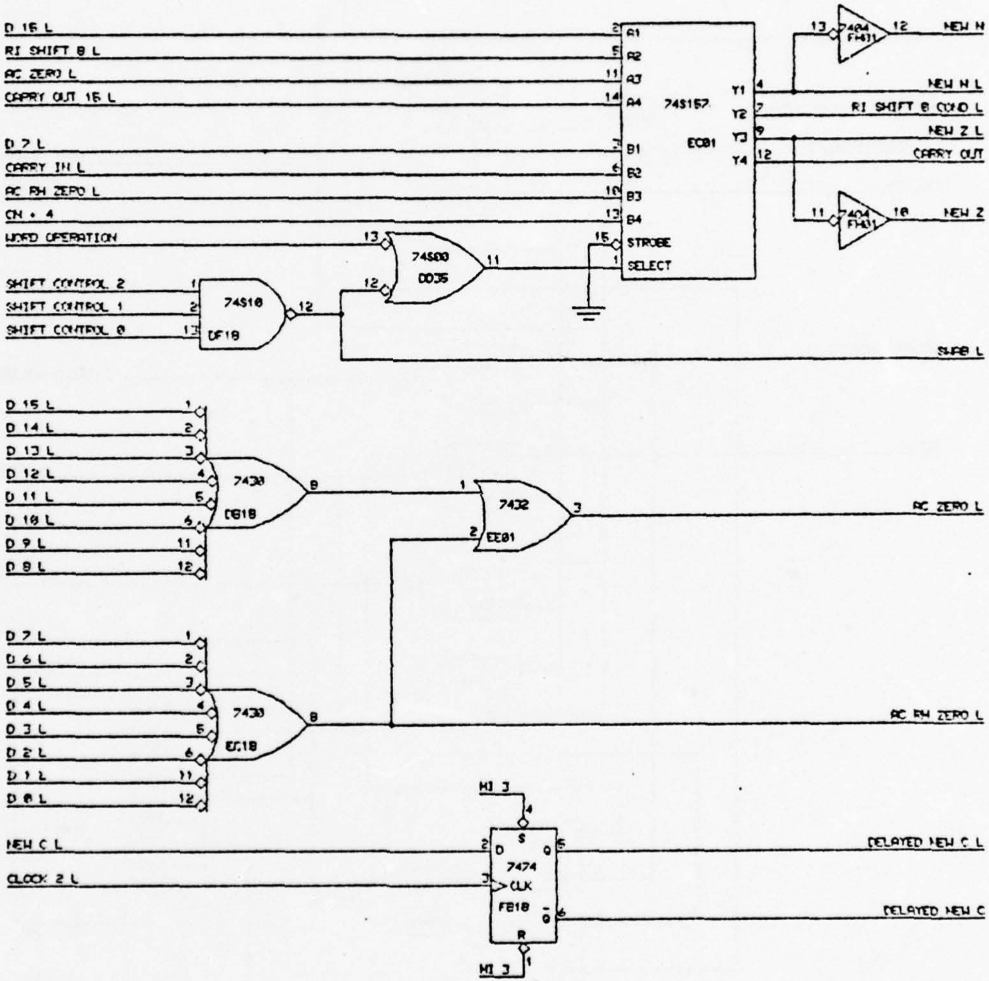

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TITLE: CONDITION CODE GENERATION

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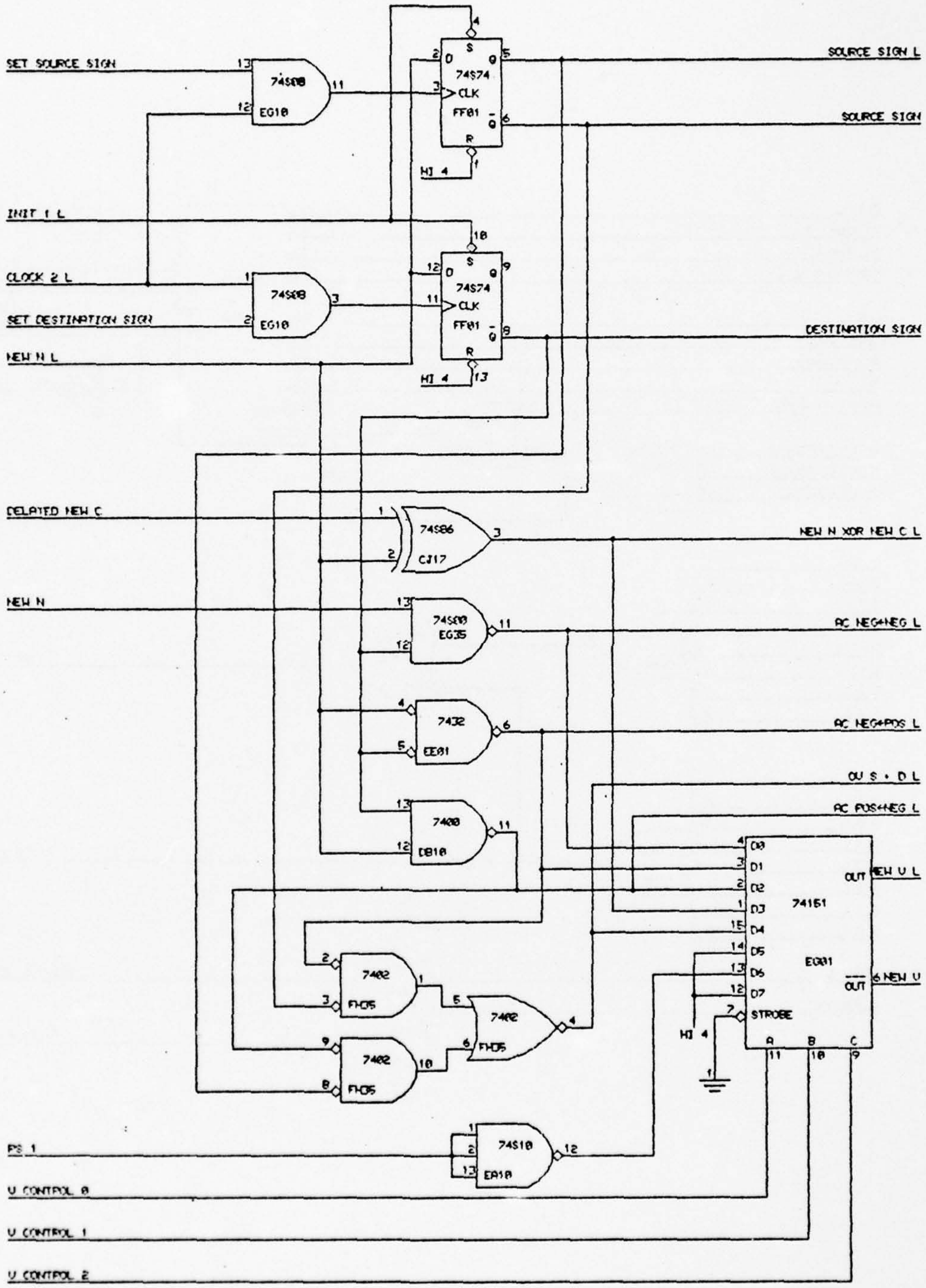

COMPUTER SCIENCE ENGINEERING LAB

TITLE: OVERFLOW LOGIC

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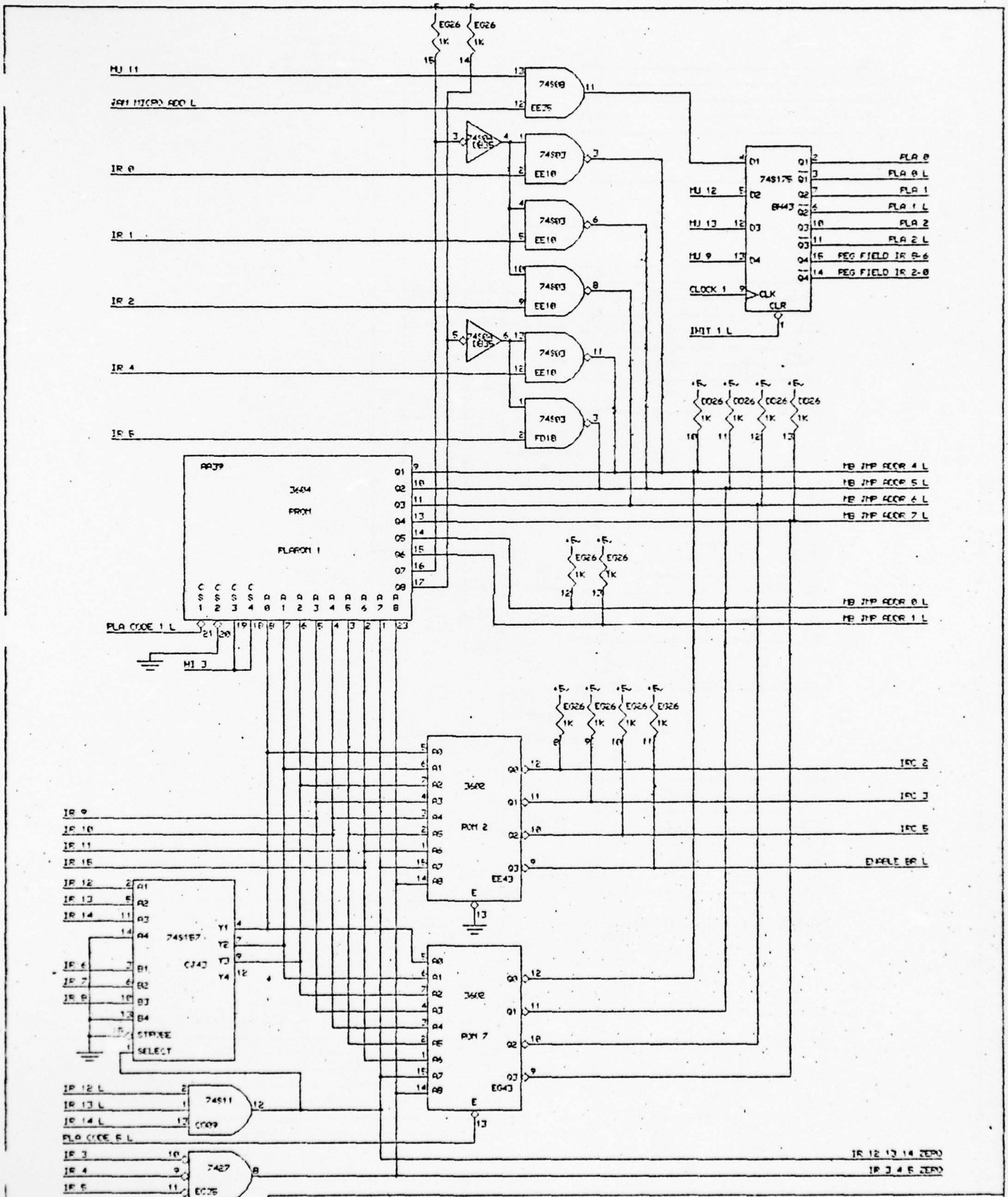

COMPUTER SCIENCE ENGINEERING LAB

TITLE: MICRO BRANCH PROMS

PROJECT:

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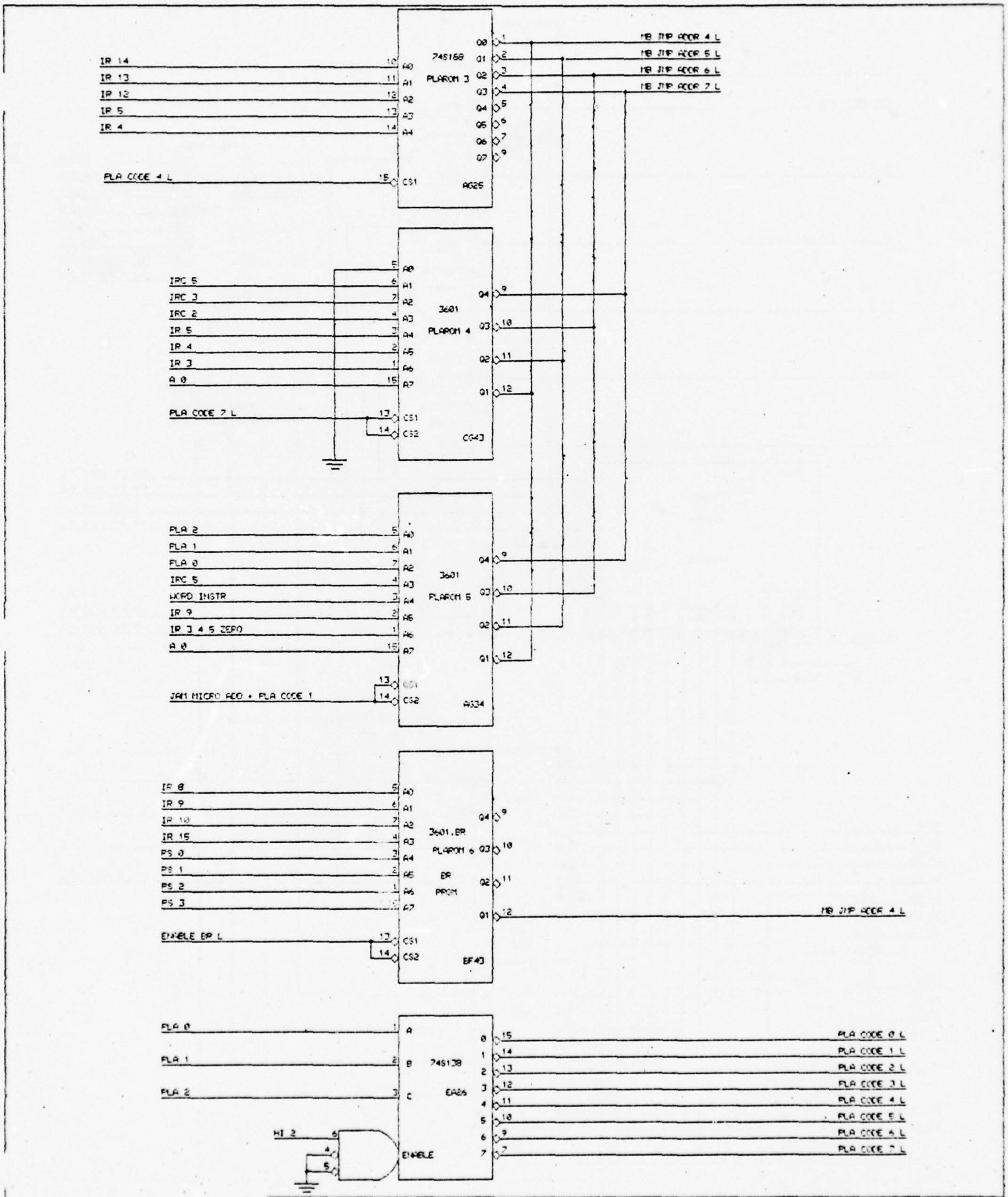
DRAWING NUMBER:

DATE: 26-JUN-75 23:02



COMPUTER SCIENCE ENGINEERING LAB

TITLE: MICRO CODE BRANCH LOGIC

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

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DRAWING FILE: NEWBR2[N210TM05]

DRAWING NUMBER:

DATE: 19-JUN-75 07:41

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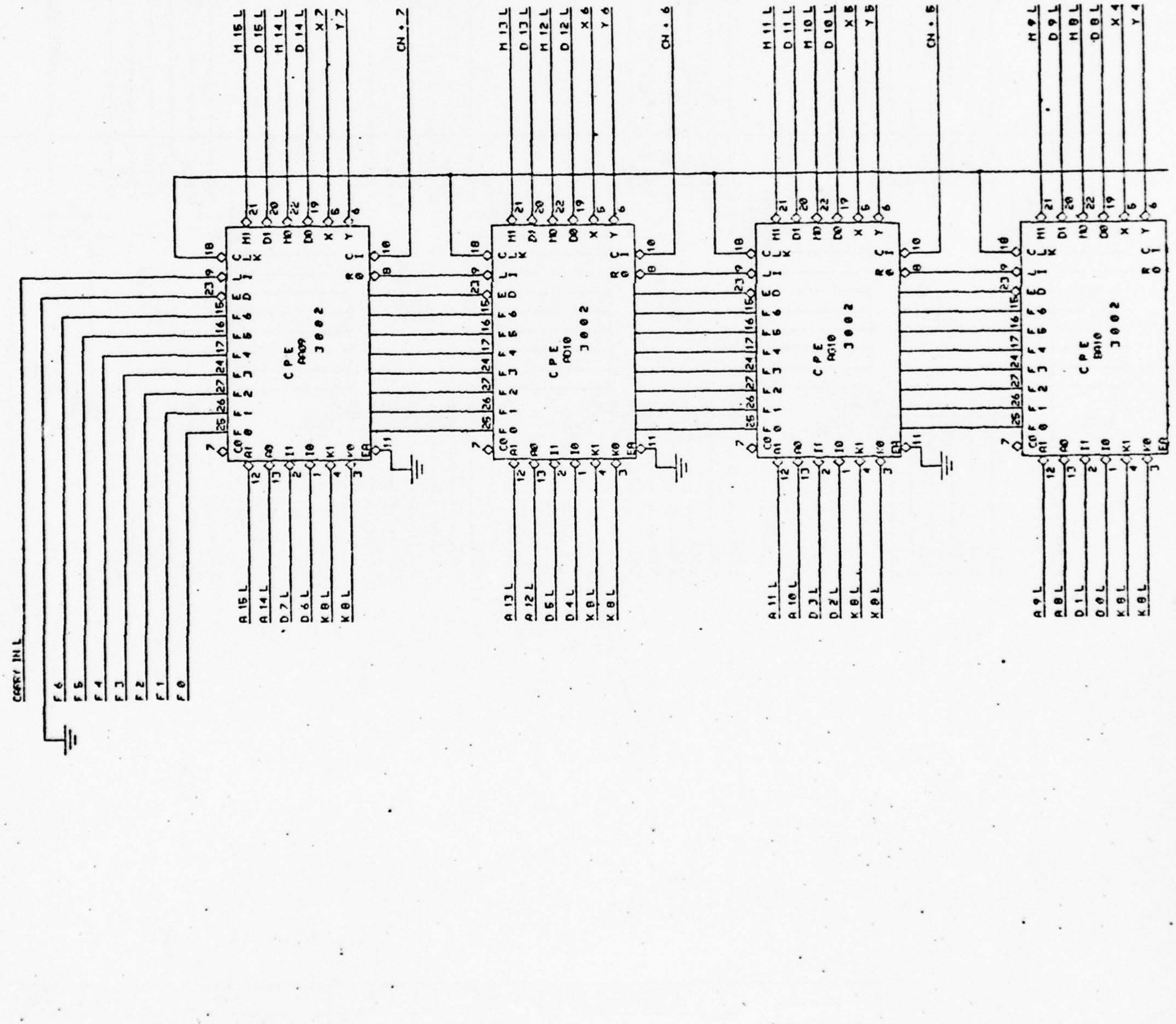
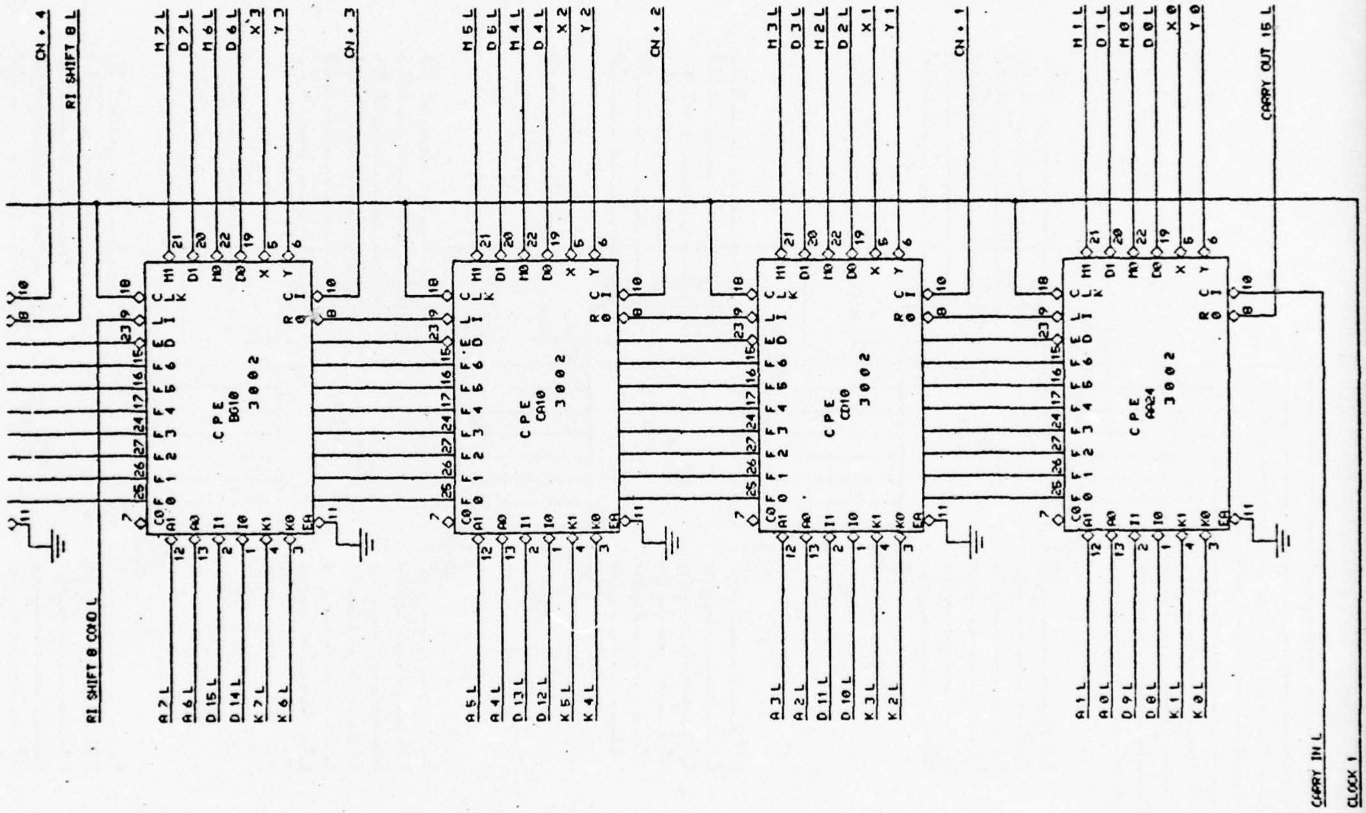

CARRY IN L
F 6
F 5
F 4
F 3
F 2
F 1
F 0
A 15 L
A 14 L
D 7 L
D 6 L
K 8 L
K 8 L
CPE AA09 3002
M 15 L
D 15 L
M 14 L
D 14 L
X 7
Y 7
CN + 7
A 13 L
A 12 L
D 5 L
D 4 L
K 8 L
K 8 L
CPE AD10 3002
M 13 L
D 13 L
M 12 L
D 12 L
X 6
Y 6
CN + 6
A 11 L
A 10 L
D 3 L
D 2 L
K 8 L
K 8 L
CPE AG10 3002
M 11 L
D 11 L
M 10 L
D 10 L
X 5
Y 5
CN + 5
A 9 L
A 8 L
D 1 L
D 0 L
K 8 L
K 8 L
CPE BB10 3002
M 9 L
D 9 L
M 8 L
D 8 L
X 4
Y 4



COMPUTER SCIENCE ENGINEERING LAB

TITLE: CENTRAL PROCESSING ELEMENT ARRAY

PROJECT:

DRAWN BY: SHERWOOD

CHECKED BY:

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DRAWING FILE: CPES[N210TM05]

DRAWING NUMBER:

DATE: 19-MAY 5 21:36

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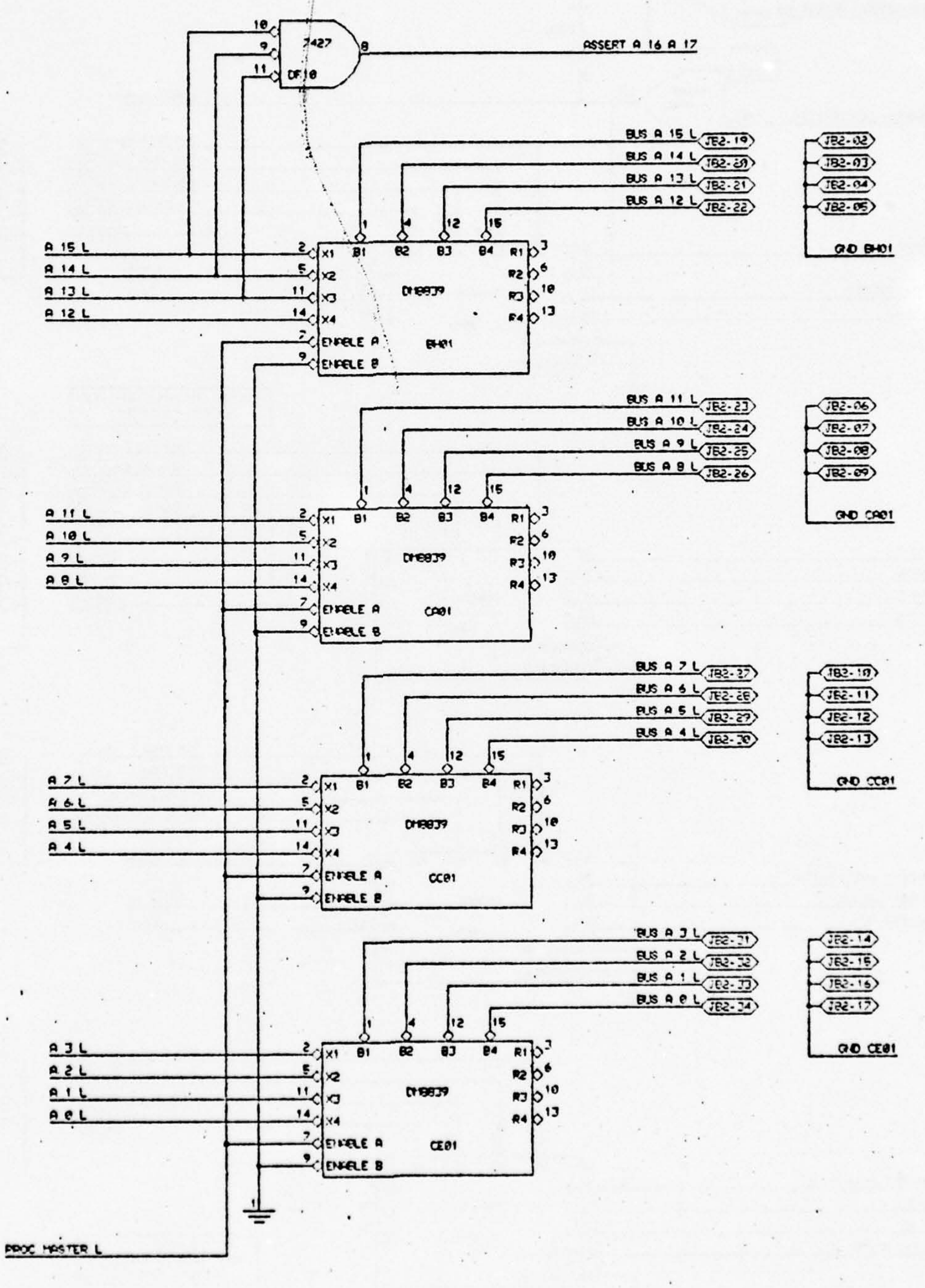

COMPUTER SCIENCE ENGINEERING LAB

TITLE: UNIBUS ADDRESS

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

CHECKED BY:

PAGE OF

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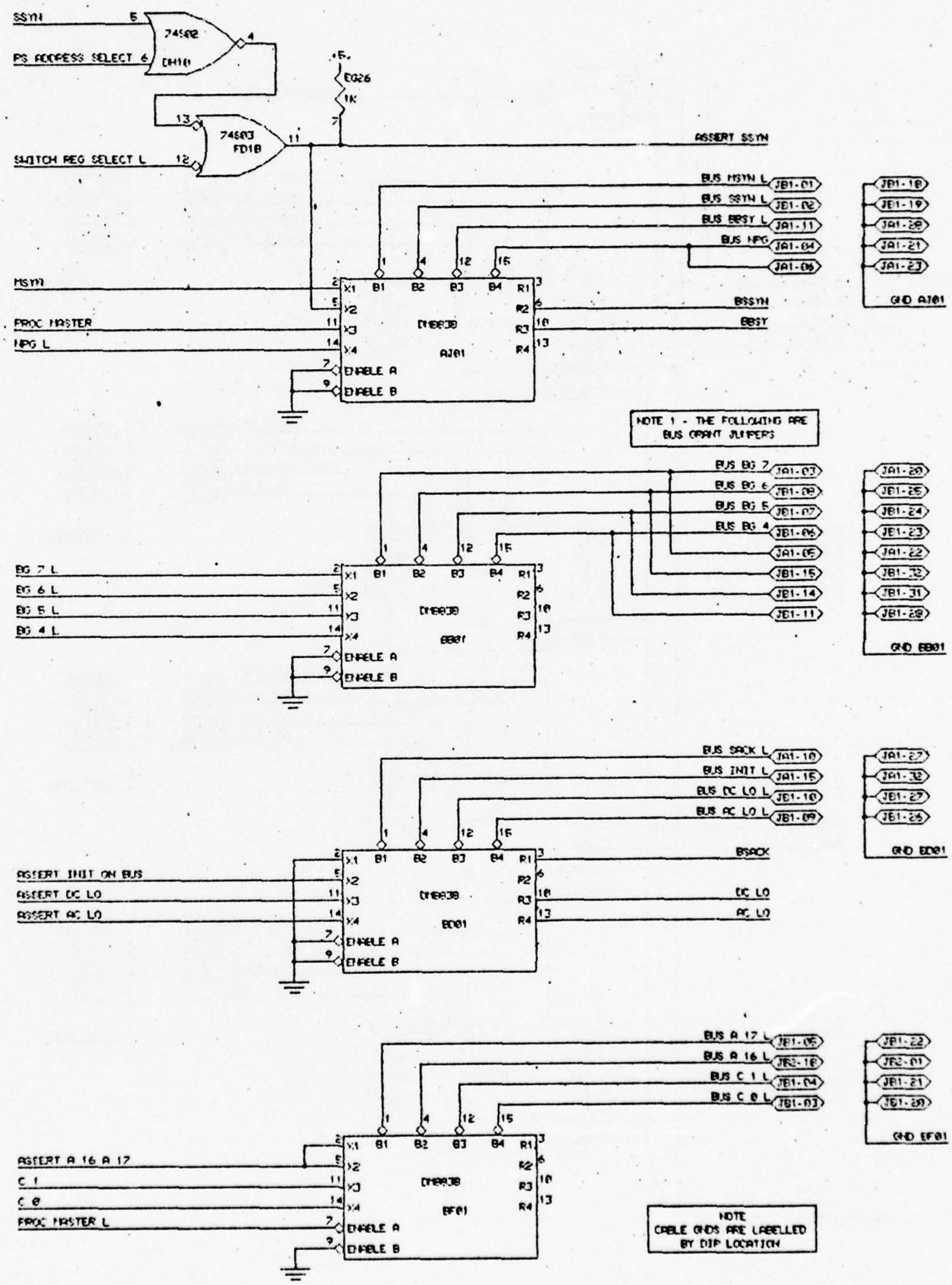
DRAWING NUMBER:

DATE: 02-JUN-75 17:46



NOTE 1 - THE FOLLOWING ARE BUS GRANT JUMPERS

NOTE
CABLE GNDS ARE LABELLED
BY DIP LOCATION

COMPUTER SCIENCE ENGINEERING LAB

TITLE: UNIBUS CONTROL LINE INTERFACE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

CHECKED BY:

PAGE OF

DRAWING FILE: UNIINT[N210TM05]

DRAWING NUMBER:

DATE: 02-JUN-75 18:02

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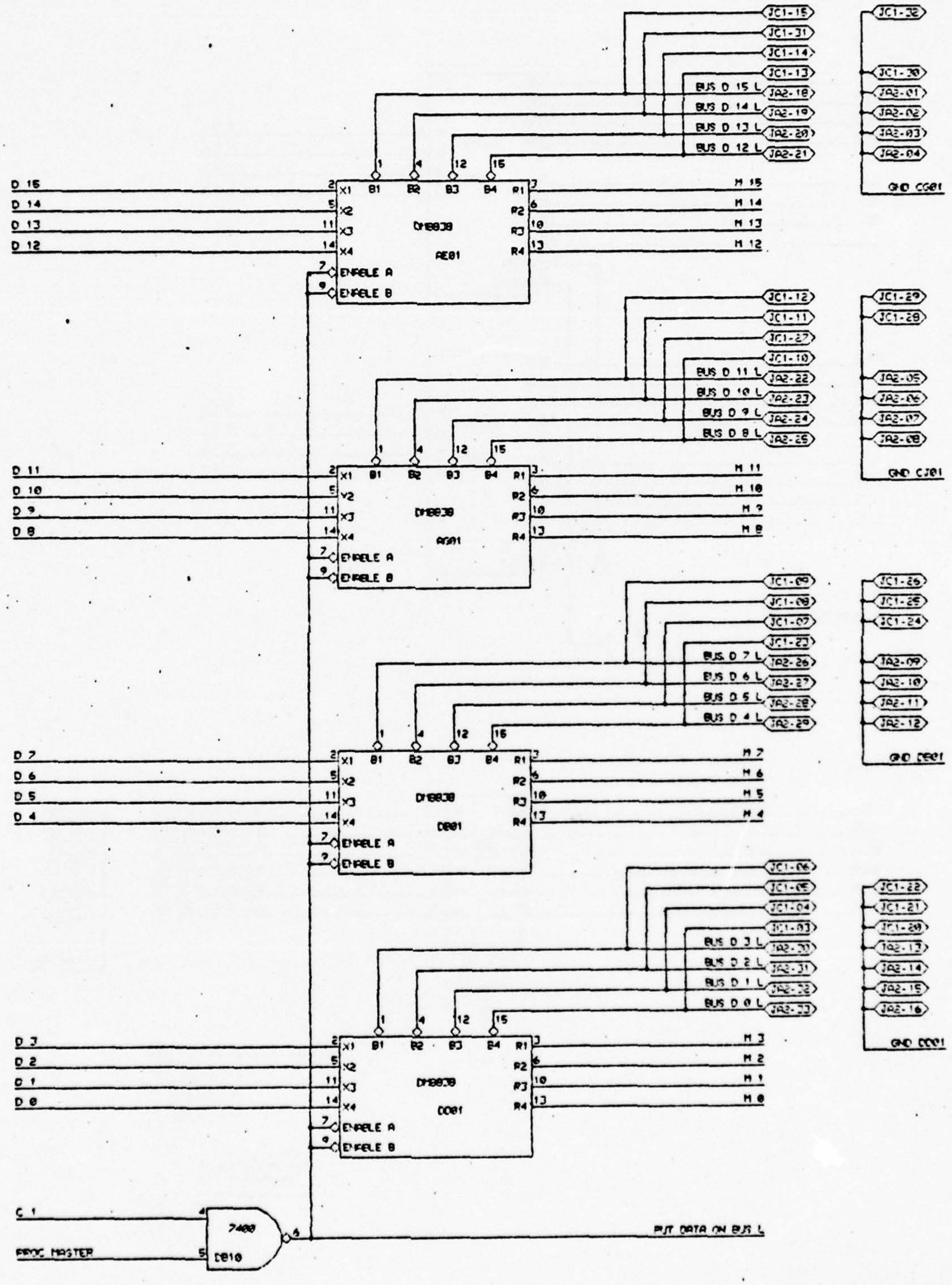

COMPUTER SCIENCE ENGINEERING LAB

TITLE: UNIBUS DATA LINES INTERFACE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

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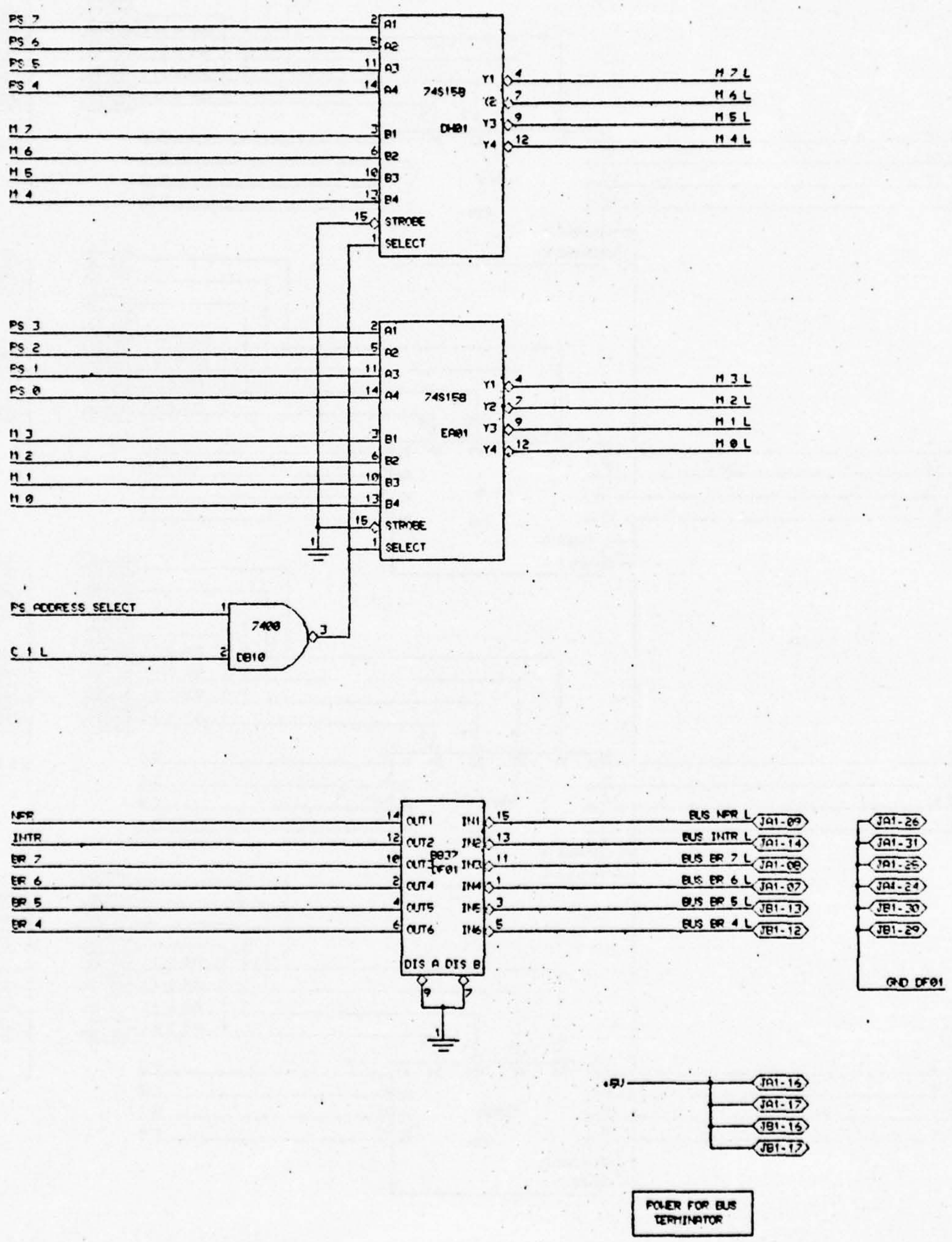

COMPUTER SCIENCE ENGINEERING LAB

TITLE: UNIBUS DATA INTERFACE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

CHECKED BY:

PAGE OF

DRAWING FILE: UNIMUX[N210TM05]

DRAWING NUMBER:

DATE: 02-JUN-75 18:06

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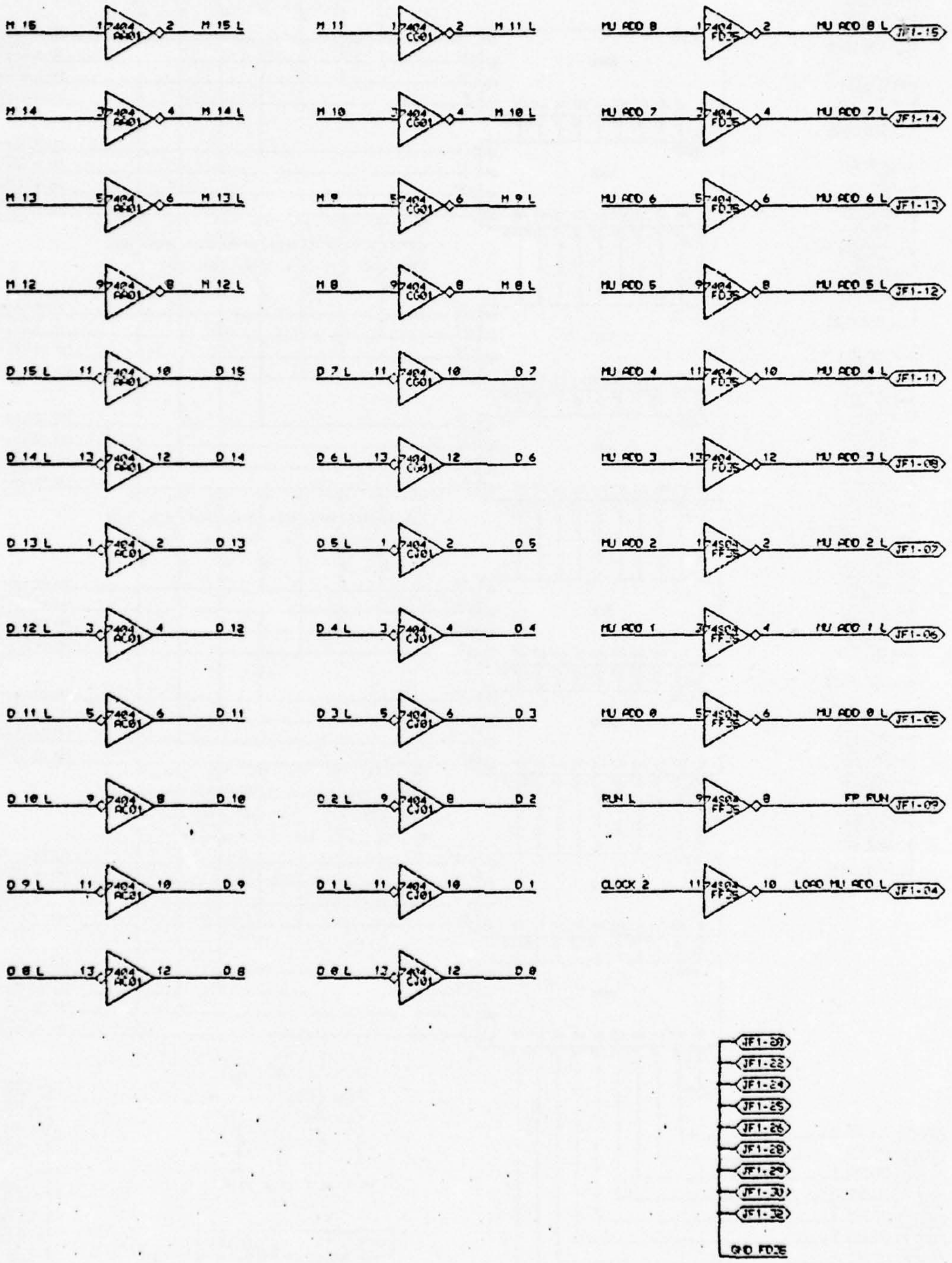
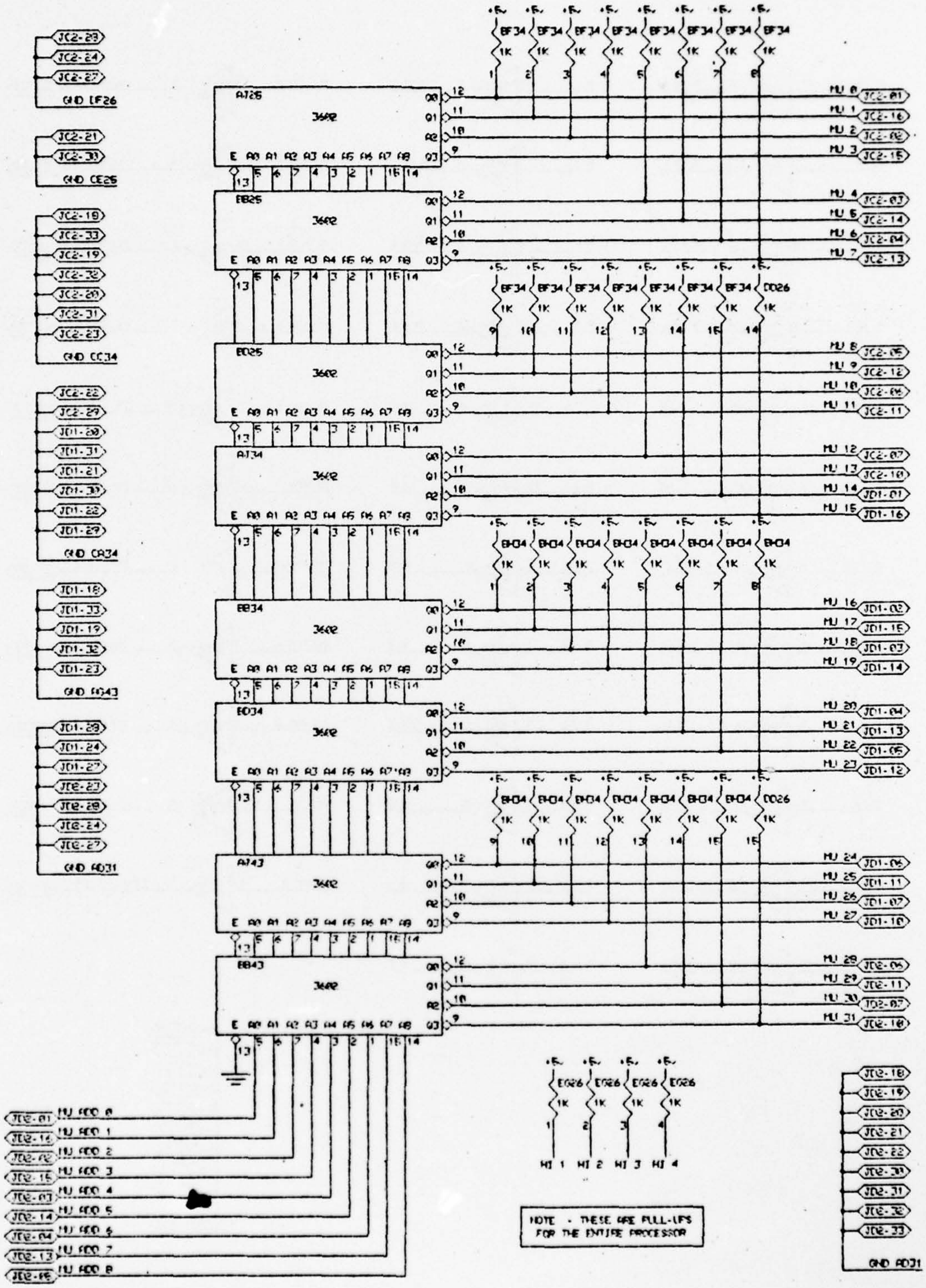

M 15 1 7404 AA01 2 M 15 L
M 14 3 7404 AA01 4 M 14 L
M 13 5 7404 AA01 6 M 13 L
M 12 9 7404 AA01 8 M 12 L
D 15 L 11 7404 AA01 10 D 15
D 14 L 13 7404 AA01 12 D 14
D 13 L 1 7404 AC01 2 D 13
D 12 L 3 7404 AC01 4 D 12
D 11 L 5 7404 AC01 6 D 11
D 10 L 9 7404 AC01 8 D 10
D 9 L 11 7404 AC01 10 D 9
D 8 L 13 7404 AC01 12 D 8
M 11 1 7404 CG01 2 M 11 L
M 10 3 7404 CG01 4 M 10 L
M 9 5 7404 CG01 6 M 9 L
M 8 9 7404 CG01 8 M 8 L
D 7 L 11 7404 CG01 10 D 7
D 6 L 13 7404 CG01 12 D 6
D 5 L 1 7404 CJ01 2 D 5
D 4 L 3 7404 CJ01 4 D 4
D 3 L 5 7404 CJ01 6 D 3
D 2 L 9 7404 CJ01 8 D 2
D 1 L 11 7404 CJ01 10 D 1
D 0 L 13 7404 CJ01 12 D 0
MU ADD 8 1 7404 FD35 2 MU ADD 8 L JF1-15
MU ADD 7 3 7404 FD35 4 MU ADD 7 L JF1-14
MU ADD 6 5 7404 FD35 6 MU ADD 6 L JF1-13
MU ADD 5 9 7404 FD35 8 MU ADD 5 L JF1-12
MU ADD 4 11 7404 FD35 10 MU ADD 4 L JF1-11
MU ADD 3 13 7404 FD35 12 MU ADD 3 L JF1-08
MU ADD 2 1 74S04 FF35 2 MU ADD 2 L JF1-07
MU ADD 1 3 74S04 FF35 4 MU ADD 1 L JF1-06
MU ADD 0 5 74S04 FF35 6 MU ADD 0 L JF1-05
RUN L 9 74S04 FF35 8 FP RUN JF1-09
CLOCK 2 11 74S04 FF35 10 LOAD MU ADD L JF1-04
JF1-20
JF1-22
JF1-24
JF1-25
JF1-26
JF1-28
JF1-29
JF1-30
JF1-32
GND FD35

COMPUTER SCIENCE ENGINEERING LAB

TITLE: INVERTERS FOR UNIBUS INTERFACE	
PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR	
DRAWN BY: SHERWOOD	CHECKED BY:
DRAWING FILE: UNI[INV[N210TM05]	DRAWING NUMBER:
PAGE OF	DATE: 12-JUN-75 03:13



COMPUTER SCIENCE ENGINEERING LAB

TITLE: PROM CONTROL STORE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

CHECKED BY:

PAGE OF

DRAWING FILE: CTLSTO[N210TM05]

DRAWING NUMBER:

DATE: 30-MAY-75 08:02

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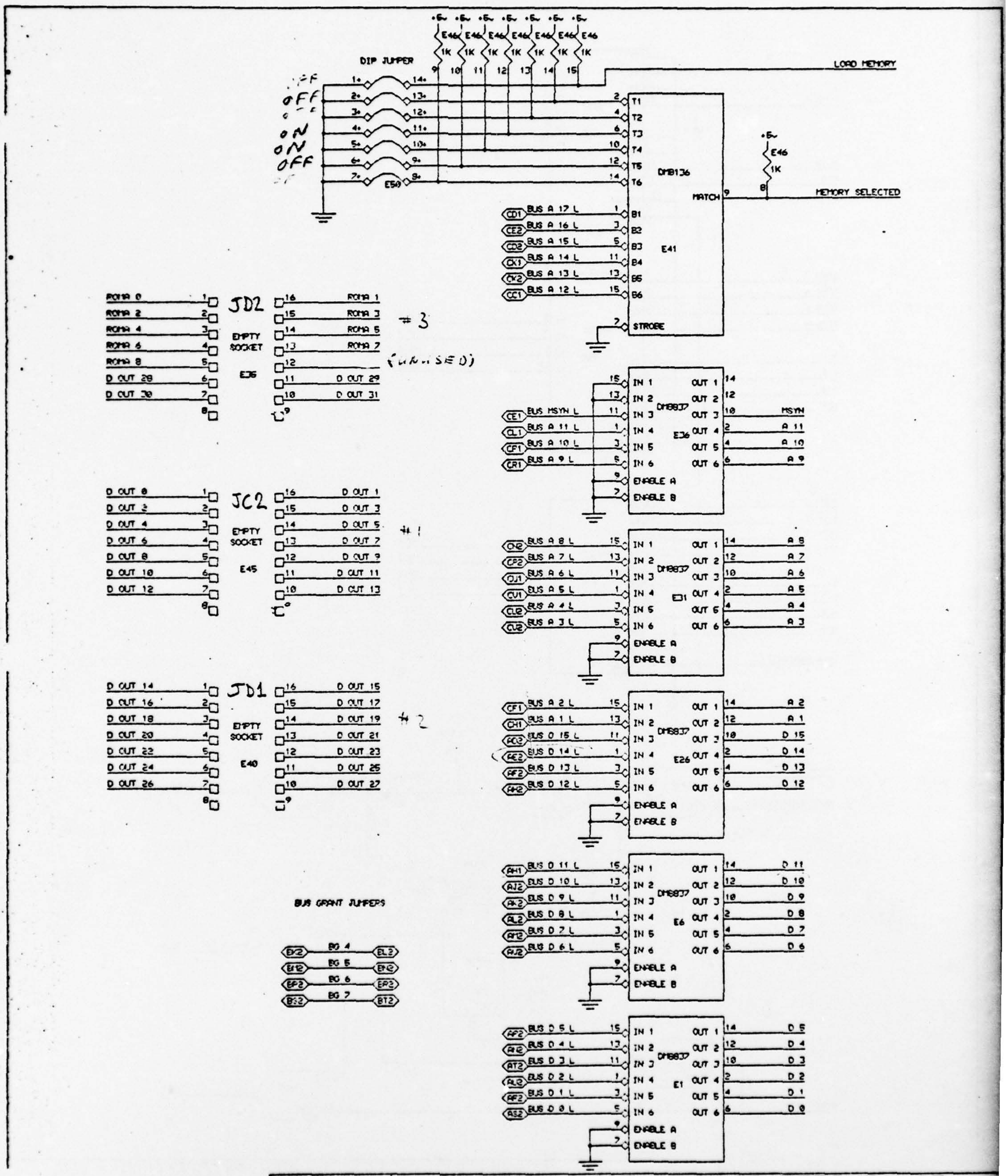

COMPUTER SCIENCE ENGINEERING LAB

TITLE: WRITEABLE CONTROL STORE - BUS INTERFACE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD | CHECKED BY: | PAGE OF

DRAWING FILE: STORE3[N210WS03] | DRAWING NUMBER: | DATE: 15-MAR-75 04:41

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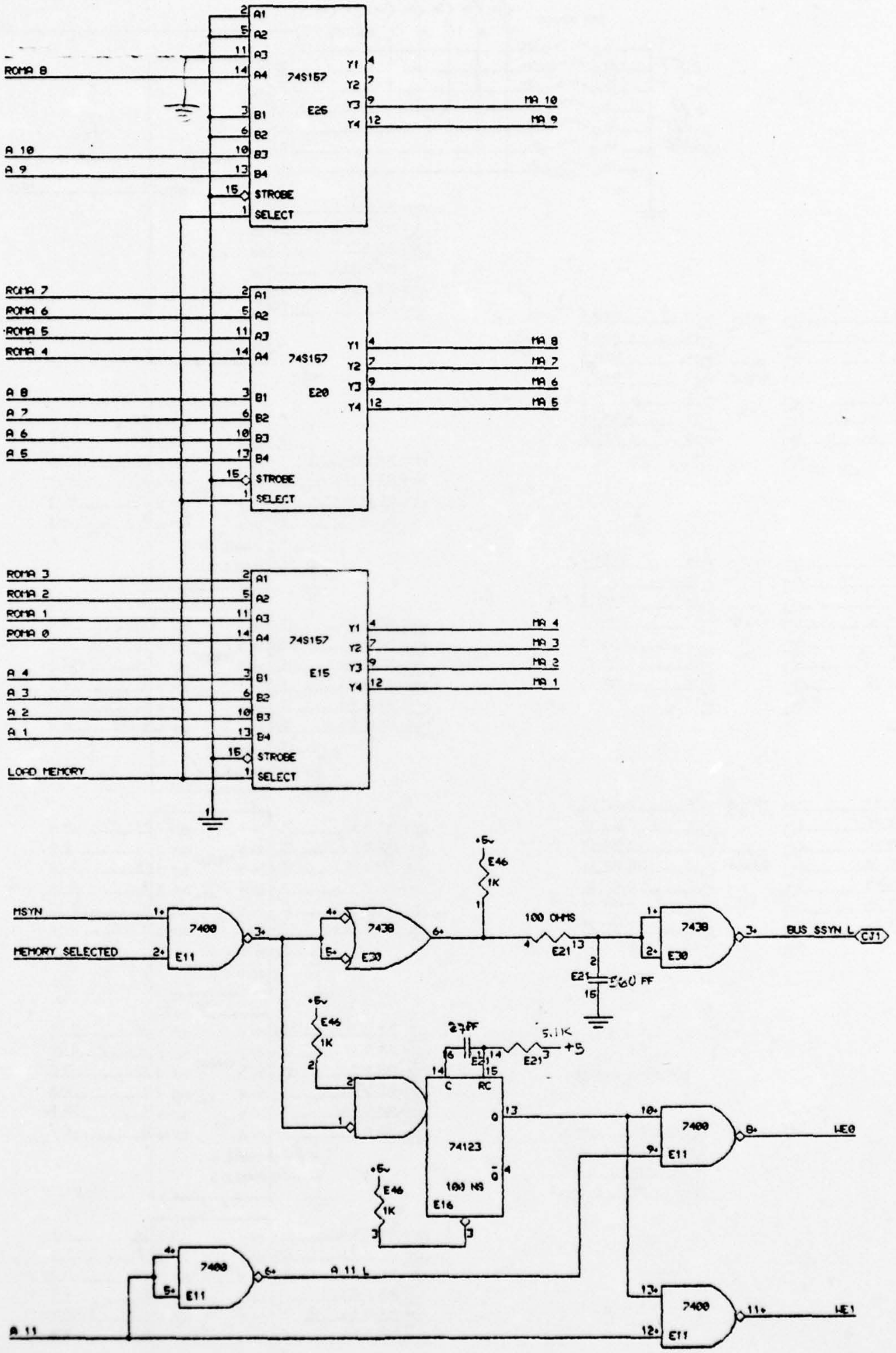

COMPUTER SCIENCE ENGINEERING LAB

TITLE:

PROJECT:

DRAWN BY: SHERWOOD

CHECKED BY:

DRAWING FILE: STORE4[N210WS03]

DRAWING NUMBER:

PAGE OF

DATE: 11-MAR-75 03:52

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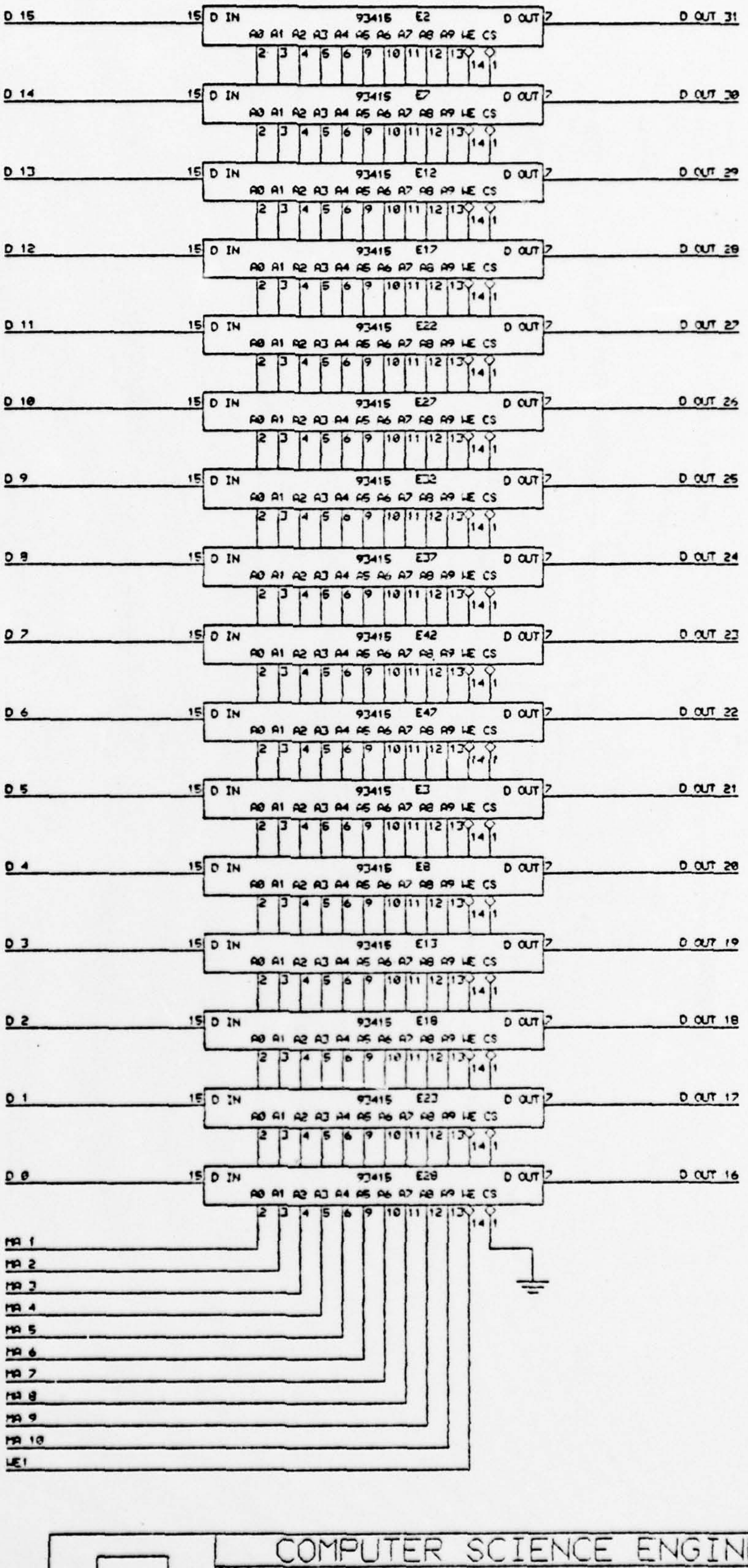

COMPUTER SCIENCE ENGINEERING LAB

TITLE: WRITEABLE CONTROL STORE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

CHECKED BY:

PAGE OF

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DRAWING NUMBER:

DATE: 10-MAR-75 22:24

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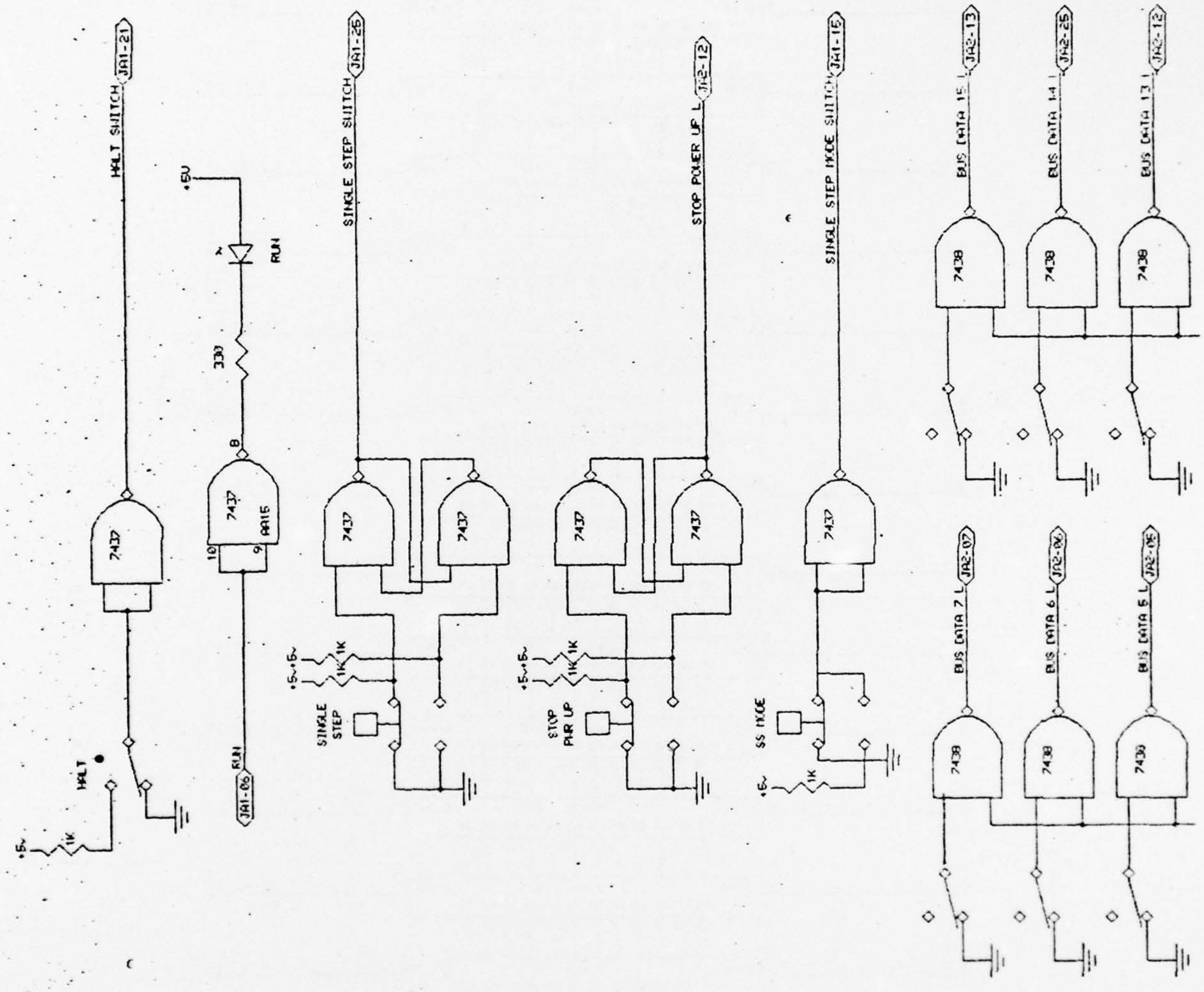
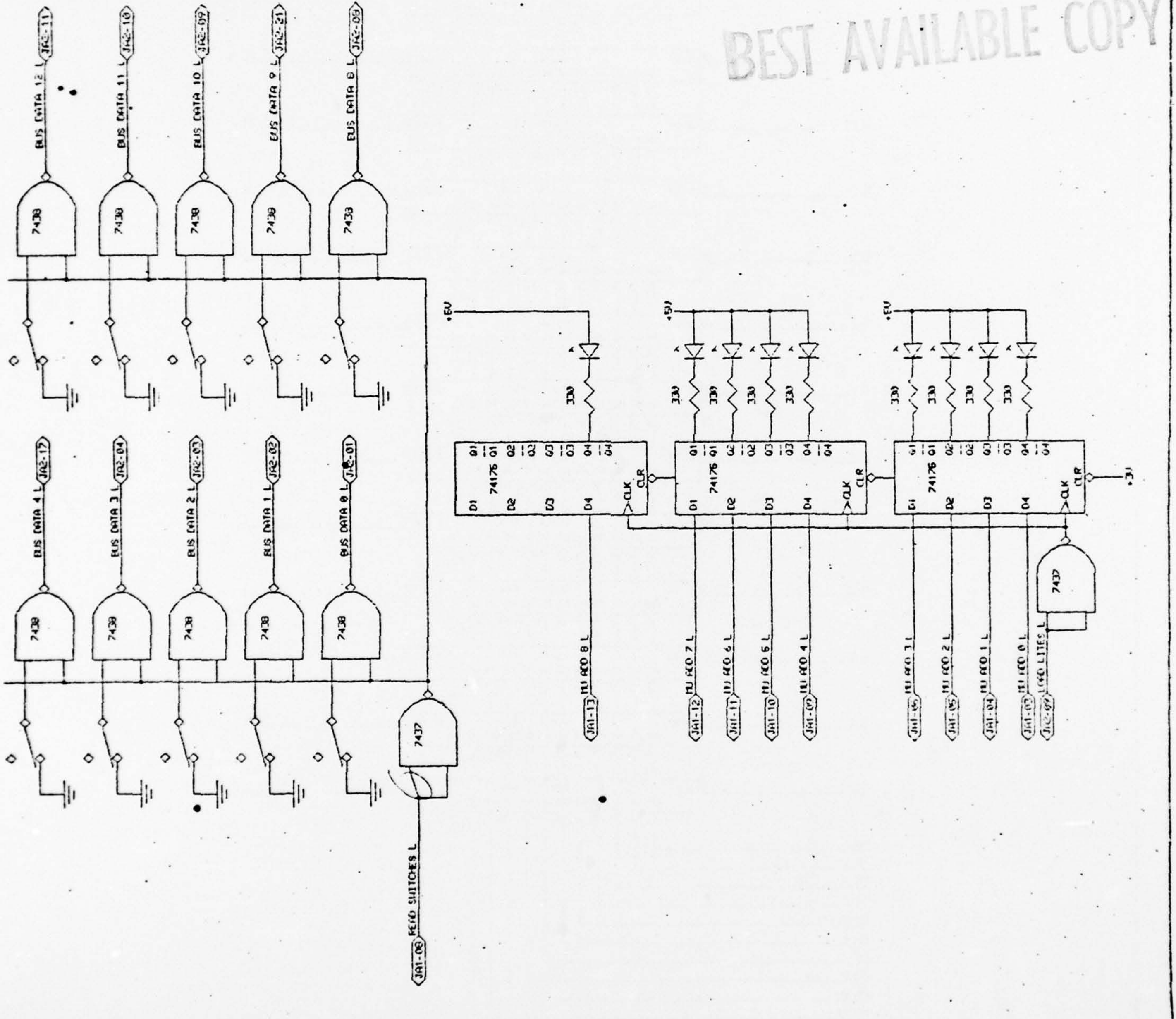

HALT SWITCH
JA1-21
7437
HALT
+5
1K
+5V
RUN
330
8
10
9
AA15
RUN
JA1-06
SINGLE STEP SWITCH
JA1-25
7437
7437
+5 +5
1K 1K
SINGLE STEP
STOP POWER UP L
JA2-12
STOP PWR UP
SINGLE STEP MODE SWITCH
JA1-15
SS MODE
BUS DATA 15 L
JA2-13
BUS DATA 14 L
JA2-25
BUS DATA 13 L
JA2-12
BUS DATA 7 L
JA2-07
BUS DATA 6 L
JA2-06
BUS DATA 5 L
JA2-05
7438



COMPUTER SCIENCE ENGINEERING LAB

TITLE: FRONT PANEL

PROJECT:

DRAWN BY:

CHECKED BY:

PAGE OF

DRAWING FILE: FPANEL[N210TM05]

DRAWING NUMBER:

DATE: 19-JUN-75 03:58

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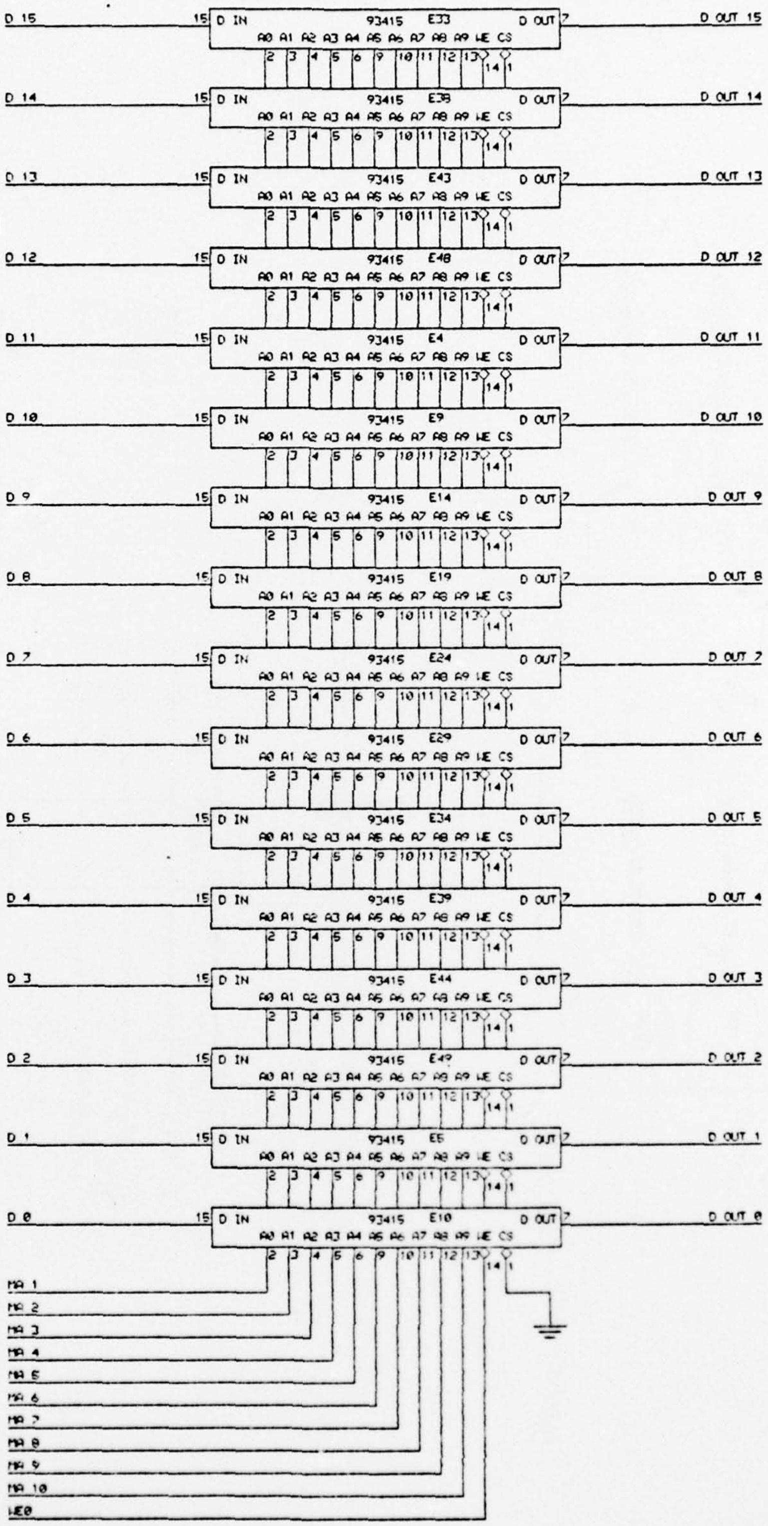

COMPUTER SCIENCE ENGINEERING LAB

TITLE: WRITEABLE CONTROL STORE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

CHECKED BY:

PAGE OF

DRAWING FILE: STORE2[N210WS03]

DRAWING NUMBER:

DATE: 10-MAR-75 22:29

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PITTSBURGH, PENNSYLVANIA 15213

```
ASSEMBLY OF MICRO.DAT ON  6-Jan-76 AT 10:48

                                                                                  ADDRESS   JMCD    OPCD   CYCD PLA KURGIMULTF

                                                                                            0000000 0011111 1111 122 2 22 22222333
                                                                                            1234567 8901234 5678 901 2 34 56789012

;--------------------------------------------------------;
;MICRO CODE TO MAKE A PDP-11/40 OUT OF THE INTEL 3000 ;
;MICRO PROCESSOR CHIPS.                                ;
;--------------------------------------------------------;
;
;
;
;PROGRAMMING CONVENTIONS USED IN CODE:
;
; 1.  ZERO IS KEPT IN R9 SO THAT TRAP ADDRESSES CAN EASILY BE
;     PUT IN IT TO CALL THE TRAP SEQUENCE.  THE TRAP SEQUENCE
;     PUTS ZERO BACK IN R9 WHEN IT IS DONE.
;
; 2.  THE Z BIT IS USED TO DETECT DOUBLE BUS ERRORS AND
;     TO INDICATE THAT THE PROCESSOR IS IN CONSOLE MODE.
;     IF IT IS SET AND A TRAP OCCURS, THE MICROPROCESSOR
;     WILL JUMP TO THE CONSOLE CODE.
;
FIELD PLA 3.0:PLA1=1,PLA2=2,PLA3=3,PLA4=4,PLA5=5,PLA6=6,PLA7=7,&
        NINST=0,INTSR=2,DECR=3,INCR=4,BUSWT=5,BREST=6,STKOV=7,&
        WIF18=4,WIF13=2
FIELD KUB 1.1:KA1=0,KL1=0                     ;NOTE: ALL K LINES ARE INVERTED.
FIELD RG12 2.3:RG1=2,RG2=0,RGD=1,KM00=3,KM01=2,KM10=1,KM11=0,&
        KTY=2,SETS1=2,SETD1=1,&
        SCLR1=1,STST1=1,SCOM1=1,SINC1=1,SDEC1=2,SNEG1=0,&
        SASR1=3,SASL1=3,SROR1=3,SROL1=3,SADC1=1,SSBC1=2,&
        SMOV1=1,SBIT1=1,SBCS1=1,SXOR1=1,SSXT1=1,SCMP1=0,&
        SSUB1=0,SADD1=0,SSWB1=3,&
        PSVS=1,PSVN=2
;
;MICRO WORD FOR I/O INSTRUCTIONS IS (8 BITS):
;  EXTENDED INSTRUCTON,GET BUS(ASSERTED LOW),PAUSE,CHECK WORD,C(1:0!,11B
;
FIELD MULTF 8.1000011B:EINS=11000011B,EGPWD=10110011B,EGWDI=10010011B,&
        EPWDI=11110011B,EWDI=11010011B,PAUSE=11000011B,EGPWT=10100011B,&
        EGDI=10000011B,EPASE=11100011B,&
        GPWDI=110011B,GPWDP=110111B,GPWDO=111011B,GPWD8=111111B,&
        GPDI=100011B,GPDIP=100111B,GPDO=101011B,GPDO8=101111B,&
        GWDI=010011B,GWDIP=010111B,GWDO=011011B,GWDO8=011111B,&
        GDI=000011B,GDIP=000111B,GDO=001011B,GDO8=001111B,&
        PWDI=1110011B,PWDIP=1110111B,PWDO=1111011B,PWDO8=1111111B,&
        PDI=1100011B,PDIP=1100111B,PDO=1101011B,PDO8=1101111B,&
        WDI=1010011B,WDIP=1010111B,WDO=1011011B,WDO8=1011111B,&
        DI=1000011B,DIP=1000111B,DO=1001011B,DO8=1001111B,&
        EDI=11000011B,EDIP=11000111B,EDO=11001011B,EDO8=11001111B,&
        K0=11111101B,KR1=01B,KN2=101B,K1=11111001B,&
        K2=11110101B,K4=11101101B,K7=11100001B,&
        K10=11011101B,K14=11001101B,K17=11000001B,K20=10111101B,&
        K21=10111001B,K24=10101101B,&
        K30=10011101B,K34=10001101B,K3S=10001001B,&
        K40=01111101B,K57=01000001B,&
        K60=111101B,K66=00100101B,K70=11101B,K71=00011001B,&
        K77=01B,KCR=11001001B,KLF=11010101B,KR8=101B,&
        KOM=01B,KZERO=00111101B,KSLSH=01000001B,&
        KTKS=111101B,KTKB=110101B,KTPS=101101B,KTPB=100101B,&
        SETSZ=2,SETDZ=2,&
        SCLRZ=01101110B,STSTZ=01101110B,SCOMZ=10101110B,&
        SINCZ=00000110B,SDECZ=00000110B,SNEGZ=10000110B,&
        SASRZ=01001110B,SASLZ=11000110B,SRORZ=01010110B,&
        SROLZ=11010110B,SADCZ=01010110B,SSBCZ=10011110B,&
        SMOVZ=00101110B,SBITZ=00101110B,SBCSZ=00101110B,&
        SXORZ=00101110B,SSXTZ=00100110B,SCMPZ=10110110B,&
        SSUBZ=10110110B,SADDZ=01101110B,SSWBZ=10111110B,&
        SETTT=00110010B,CLRTT=10110010B,SSWB3=00111010B,&
        PSCS=01111110B,PSCN=00111110B,PSCIN=00010010B
;
;----------------------------------------------;
;PUT RESULT OF LAST INSTRUCTION IN MEMORY      ;
;AND FETCH NEXT INSTRUCTION.                   ;
;----------------------------------------------;
;
4   WDESR:  SDR R0,1,KA1,RG2,JMP FETCH  ;4 R(N)=AC                    /00072/   000000100 0101011 0100000 1111 000 0 00 01000011
;
6   WDSRB:  SDR T,1,KM11,K77            ;6 T=AC AND 377               /00074/   000000110 0011101 0101100 1111 000 1 00 00000001
470         ILR R0,RG2                  ;726 AC=R(NZ)                 /00075/   111010110 0010010 0000000 0011 000 1 00 01000011
294         ILR T,KL1,K0                ;446 AC,T=T+(AC AND 177400)   /00076/   100100110 0011000 0001100 0011 000 0 11 11111101
390         SDR R0,1,KA1,RG2,JMP FETCH  ;606 R(NZ)=AC                 /00077/   110000110 0101011 0100000 1111 000 0 00 01000011
;
0   WDESW:  NOP GPWDO,JMP FETCH         ;0 M(MAR)=AC                  /00079/   000000000 0101011 0001101 0011 000 1 11 00111011
;
1   ODDAD:  LMI R9,K4,JMP GTRAP         ;1 TRAP TO LOC 4              /00081/   000000001 0101010 0011001 0011 000 1 11 11101101
```

```
                                    ;ODD ADDRESSING ERROR.
;
3   WDEOB:  LDI AC.1.KA1            ;3 ODD BYTE, SWAP HALVES      /00084/   000000011 0100010 0101111 1111 000 0 11 01000011
2   WDESB:  NOP GPDOB.JMP FETCH     ;2 M(MAR)=AC, BYTE            /00085/   000000010 0101011 0001101 0011 000 1 11 00101111
;
;
11  FETCH:  LMI R7.EGDI             ; MAR=R(7)                    /00088/   000001011 0100111 0010111 0011 000 1 11 10000011
7   FFET:   ADR R7.1.EINS           ;7 R(7)=R(7)+1                /00089/   000000111 0010110 0110111 1111 000 1 11 11000011
359         AMA T.EPWDI             ;547 T=INSTRUCTION            /00090/   101100111 0111110 0001010 0011 000 1 11 11110011
366         ADR R7.1.PLA1           ;556 WAIT FOR INSTPUCTION DECOD/00091/  101101110 0010101 0110111 1111 001 1 11 01000011
350         LMI R7.0 STZ.PLA7.JMP 350  ;536 DO INITIAL DECODE     /00092/   101011110 0010101 0010111 0001 111 1 11 01000011
                                    ;ON INSTRUCTION BY USING THE
                                    ;MICRO INTERRUPT FEATURE.
                                    ;MAR=R7,Z=0
;
;----------------------------------------------------;
;LOAD SOUPCE OPERAND INTO T.  FORMAT IS SSDD          ;
;INSTPUCTION CLASS 1                                  ;
;----------------------------------------------------;
;
;PEGISTER MODE=0: R(N)
;
80  SOP0:   ILR R0.RG1.PLAZ         ;120 AC=R(N)                  /00104/   001010000 0111100 0000000 0011 010 1 10 01000011
92          NOP PLA4.JPX 64         ;132                          /00105/   001011100 1111000 0001101 0011 100 1 11 01000011
;
;REGISTER MODE=1:  (R(N))+
;
81  SOP1:   LMI R0.RG1.EGDI.INCR    ;121 MAR=R(N), R(N)=R(N)+CONDIN/00109/  001010001 0111011 0010000 0011 100 1 10 10000011
91          ILR R0.1.RG1.PLAZ.JMP SRCMR ;R(N),AC=R(N)+1           /00110/   001011011 0111101 0000000 1111 010 1 10 01000011
;
;REGISTER MODE=2:  -(R(N))
;
82  SOP2:   LMI R0.KA1.RG1          ;122 R(N)=R(N)-1              /00114/   001010010 0011010 0010000 0011 000 0 10 01000011
418         LMI R0.KA1.PG1.EINS.DECR    ;R(N)=R(N)-1+CONDDECR     /00115/   110100010 0111101 0010000 0011 011 0 10 11000011
429         LMI R0.RG1.GDI.JMP SRCM1 ;MAR=R(N)                    /00116/   110101101 0010100 0010000 0011 000 1 10 00000011
;
;PEGISTER MODE=3: X(R(N))
;
83  SOP3:   LMI R7.1.GWDI           ;123 MAR=R(7), R(7)=R(7)+1,   /00120/   001010011 0111111 0010111 1111 000 1 11 00010011
95          ILR R7.1.WDI            ;R(7)=R(7)+1                  /00121/   001011111 0010001 0000111 1111 000 1 11 01010011
287         ILR R0.RG1.WDI             ;AC=R(N1)                  /00122/   100011111 0111110 0000000 0011 000 1 10 01010011
286         AMA AC.KA1.PWDI         ;AC=AC+M(MAR)                 /00123/   100011110 0010100 0001011 0011 000 0 11 01110011
334         LMI AC.GDI              ;MAR=AC                       /00124/   101001110 0111101 0011101 0011 000 1 11 00000011
333 SRCM1:  NOP PLAZ.DI               ;ALLOWS ADDR LINES TO SETTLE /00125/  101001101 0000101 0001101 0011 010 1 11 01000011
93  SRCMR:  LTM AC.KA1.PDI.PLA4.JPX 64  ;135 AC=M(MAR)            /00126/   001011101 1111000 1011011 0011 100 0 11 01100011
;
65  SIRB:   SDR T.1.KA1.PLA7.SETS1.SETS2.JPX 64                   /00128/   001000001 1111000 0101100 1111 111 0 10 00000010
                                    ;101 GO CALCULATE SECOND OPERAND
                                    ;PUT SOURCE OPERAND INTO T AND
                                    ;SET SOURCE SIGN BIT.
;
;INDIRECT BIT SET
;
66  SDEF:   LMI AC.GDI              ;102 MAR=AC                   /00135/   001000010 0010000 0011101 0011 000 1 11 00000011
258         NOP DI                  ;NEEDED TO DO ADDRESSING      /00136/   100000010 0111110 0001101 0011 000 1 11 01000011
270         LTM AC.KA1.PLA3.PDI                                   /00137/   100001110 0000101 1011011 0011 011 0 11 01100011
94          NOP PLA4.JPX 64         ;T=M(MAR)                     /00138/   001011110 1111000 0001101 0011 100 1 11 01000011
;
67  SOBYT:  LDI AC.1.KA1.PLA4.JMP SIRB  ;103 AC=AC SWAPPED        /00140/   001000011 0110001 0101111 1111 100 0 11 01000011
;
;------------------------------------------------;
;LOAD DESTINATION'S OPGINAL VALUE INTO AC IF USED ;
;IN INSTRUCTION.                                  ;
;INSTRUCTION CLASS 2                              ;
;------------------------------------------------;
;
;REGISTER MODE=0:  R(N)
;
68  DUSE0:  ILR R0.RGZ.JPX DUIRB     ;104 AC=R(NZ)                /00150/   001000100 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1: (R(N))+
;
69  DUSE1:  LMI R0.1.RGZ.GDIP       ;105 MAR=R(N), R(N)=R(N)+1,   /00154/   001000101 0011001 0010000 1111 000 1 00 00000111
405         ILR R0.RGZ.EDIP.INCR     ;R(N),AC=R(N)+CONDINCR       /00155/   110010101 0110110 0000000 0011 100 1 00 11000111
406         NOP PLA7.DIP.JMP DESMR                                /00156/   110010110 0000111 0001101 0011 111 1 11 01000111
;
;REGISTER MODE=2:  -(R(N))
;
70  DUSE2:  LMI R0.KA1.RGZ          ;106 R(N)=R(N)-1              /00160/   001000110 0011011 0010000 0011 000 0 00 01000011
438         LMI R0.KA1.RGZ.EINS.DECR  ;666 R(N)=R(N)-1+CONDDECR   /00161/   110110110 0010100 0010000 0011 011 0 00 11000011
326         LMI R0.RGZ.GDIP.JMP DESM1  ;526 MAR=R(N)              /00162/   101000110 0011010 0010000 0011 000 1 00 00000111
;
;REGISTER MODE=3:  X(R(N))
;
71  DUSE3:  LMI R7.1.GWDI           ;107 MAR=R(7), R(7)=R(7)+1    /00166/   001000111 0010101 0010111 1111 000 1 11 00010011
343         ILR R7.1.WDI            ;R(7)=R(7)+1                  /00167/   101010111 0110101 0000111 1111 000 1 11 01010011
341         ILR R0.RGZ.WDI          ;AC=R(NZ)                     /00168/   101010101 0010110 0000000 0011 000 1 00 01010011
357         AMA AC.KA1.PWDI         ;AC=AC+M(MAR)                 /00169/   101100101 0110110 0001011 0011 000 0 11 01110011
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358          LMI AC.GDIP                  ;546 MAR=AC                   /00170/   101100110 0011010 0011101 0011 000 1 11 00000111
422 DESM1:   NOP PLA7.DIP                 ;ALLOWS ADDR LINES TO SETTLE  /00171/   110100110 0000111 0001101 0011 111 1 11 01000111
118 DESMR:   LTM AC.KA1.WIF13.PDIP.JPX DUIRB                            /00172/   001110110 1111011 1011011 0011 010 0 11 01100111
                                  ;166 AC=M(MAR)
;
112 DUIRB:   NOP SETD1.SETD2.PLA5         ;160 JUMP TO INSTRUCTIONS ADC. /00175/  001110000 0101101 0001101 0011 101 1 01 00000010
13  DUIB1:   NOP JPX ADC                  ;15                           /00176/   000001101 1111001 0001101 0011 000 1 11 01000011
;
;INDIRECT BIT SET
;
113 DUDEF:   NOP GDO                      ;161 DIP MUST BE FOLLOWED BY A D/00180/ 001110001 0011000 0001101 0011 000 1 11 00001011
385          NOP                          .                             /00181/   110000001 0111011 0001101 0011 000 1 11 01000011
395          NOP PDO                                                    /00182/   110001011 0000111 0001101 0011 000 1 11 01101011
123 DUDFR:   LMI AC.GDIP.PLA6             ;173 MAR=AC                   /00183/   001111011 0111100 0011101 0011 110 1 11 00000111
124          LTM AC.KA1.PDIP.JPX DUIRB                                  /00184/   001111100 1111011 1011011 0011 000 0 11 01100111
;
114 DUOB:    LDI AC.1.KA1.PLA5.JMP DUIB1 ;162 ODD BYTE                  /00186/   001110010 0101101 0101111 1111 101 0 11 01000011
;
;-------------------------------------------------------;
;CALCULATE DESTINATION'S ADDRESS AND PUT IT IN MAR AND AC;
;INSTRUCTION CLASS 3                                    ;
;-------------------------------------------------------;
;
;REGISTER MODE=0: R(N)
;
72  DA0:     ILR R0.RG2;JPX DUIRB         ;110 AC=R(N)                  /00195/   001001000 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1:  (R(N))+
;
73  DA1:     ILR R0.RG2                   ;111 AC=R(N)                  /00199/   001001001 0011100 0000000 0011 000 1 00 01000011
457          ADR R0.RG2.EINS.INCR         ;R(N)=R(N)+CONDINCR           /00200/   111001001 0111111 0110000 0011 100 1 00 11000011
463          ADR R0.1.RG2.PLA7            ;R(N)=R(N)+1                  /00201/   111001111 0000111 0110000 1111 111 1 00 01000011
127 JDURB:   LMI AC.JPX DUIRB             ;177 MAR=AC                   /00202/   001111111 1111011 0011101 0011 000 1 11 01000011
;
;REGISTER MODE=2:  -(R(N))
;
74  DA2:     LMI R0.KA1.RG2               ;112 R(N)=R(N)-1              /00206/   001001010 0000011 0010000 0011 000 0 00 01000011
58           LMI R0.KA1.RG2.EINS.DECR     ;R(N)=R(N)-1+CONDECR          /00207/   000111010 0111111 0010000 0011 011 0 00 11000011
63           ILR R0.RG2.PLA7.JMP JDURB    ;AC=R(N)                      /00208/   000111111 0000111 0000000 0011 111 1 00 01000011
;
;REGISTER MODE=3:  X(R(N))
;
75  DA3:     LMI R7.1.GWDI                ;113 MAR=R(7). R(7)=R(7)+1.   /00212/   001001011 0000010 0010111 1111 000 1 11 00010011
43           ADR R7.1.WDI                 ;R(7)=R(7)+1                  /00213/   000101011 0111100 0110111 1111 000 1 11 01010011
44           ILR R0.RG2.WDI               ;AC=R(N2)                     /00214/   000101100 0111111 0000000 0011 000 1 00 01010011
47           AMA AC.KA1.PLA7.PWDI.JMP JDURB       ;AC=AC+M(MAR)         /00215/   000101111 0000111 0001011 0011 111 0 11 01110011
;
116 DAIRB:   NOP SETD1.SETD2.PLA5         ;164                          /00217/   001110100 0101001 0001101 0011 101 1 01 00000010
9            NOP JPX SXT          ;JUMP TO INSTRUCTIONS SXT, ...        /00218/   000001001 1111010 0001101 0011 000 1 11 01000011
;
;INDIRECT BIT SET
;
117 DADEF:   AMA AC.GPWDI                         ;165                  /00222/   001110101 0111110 0001011 0011 000 1 11 00110011
126 DADFR:   LMI AC.JMP DAIRB             ;MAR=AC                       /00223/   001111110 0110100 0011101 0011 000 1 11 01000011
;
;-----------------------------------------;
;LOAD SOURCE OPERAND INTO AC.  FORMAT IS SS ;
;INSTRUCTION CLASS 5                      ;
;-----------------------------------------;
;
;REGISTER MODE=0: R(N)
;
76  LSOP0:   ILR R0.RG2.JPX DUIRB         ;114 AC=R(N)                  /00232/   001001100 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1:  (R(N))+
;
77  LSOP1:   LMI R0.RG2.EGDI.INCR         ;115 MAR=R(N). R(N)=R(N)+CONDIN/00236/  001001101 0000111 0010000 0011 100 1 00 10000011
125          ILR R0.1.RG2.DI.PLA7.JMP LSCMR ;R(N).AC=R(N)+1             /00237/   001111101 0110111 0000000 1111 111 1 00 01000011
;
;REGISTER MODE=2:  -(R(N))
;
78  LSOP2:   LMI R0.KA1.RG2               ;116 R(N)=R(N)-1              /00241/   001001110 0010011 0010000 0011 000 0 00 01000011
318          LMI R0.KA1.RG2.EINS.DECR     ;R(N)=R(N)-1+CONDECR          /00242/   100111110 0011101 0010000 0011 011 0 00 11000011
478          LMI R0.RG2.GDI.JMP LSCM1 ;MAR=R(N)                         /00243/   111011110 0110111 0010000 0011 000 1 00 00000011
;
;REGISTER MODE=3: X(R(N))
;
79  LSOP3:   LMI R7.1.GWDI                ;117 MAR=R(7). R(7)=R(7)+1.   /00247/   001001111 0010110 0010111 1111 000 1 11 00010011
367          ILR R7.1.WDI                 ;R(7)=R(7)+1                  /00248/   101101111 0111101 0000111 1111 000 1 11 01010011
365          ILR R0.RG2.WDI               ;AC=R(N2)                     /00249/   101101101 0011000 0000000 0011 000 1 00 01010011
397          AMA AC.PWDI.KA1              ;AC=AC+M(MAR)                 /00250/   110001101 0110111 0001011 0011 000 0 11 01110011
391          LMI AC.GDI                   ; MAR=AC                      /00251/   110000111 0011101 0011101 0011 000 1 11 00000011
471 LSCM1:   NOP PLA7                     ;ADDR LINES SETTLE            /00252/   111010111 0000111 0001101 0011 111 1 11 01000011
119 LSCMR:   LTM AC.KA1.WIF13.PDI.JPX DUIRB       ;167 AC=M(MAR)        /00253/   001110111 1111011 1011011 0011 010 0 11 01100011
;
120 LSIRB:   NOP SETD1.SETD2.PLA5         ;170 JUMP TO INSTRUCTIONS TST. /00255/  001111000 0101100 0001101 0011 101 1 01 00000010
12  LSIB1:   LMI R7.JPX TST               ;14 MAR=PC                    /00256/   000001100 1111011 0010111 0011 000 1 11 01000011
;
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;INDIRECT BIT SET
;
121 LSDEF:  LMI AC.GDI                 ;171 MAR=AC                   /00260/   001111001 0110011 0011101 0011 000 1 11 00000011
115         NOP DI.PLA6                ;ADDR LINES SETTLE            /00261/   001110011 0000110 0001101 0011 110 1 11 01000011
99          LTM AC.KA1.PDI.JPX DUIRB                                 /00262/   001100011 1111011 1011011 0011 000 0 11 01100011
;
122 LSOB:   LDI AC.1.KA1.PLAS.JMP LSIB1 ;172 ODD BYTE - SWAP AC      /00264/   001111010 0101100 0101111 1111 101 0 11 01000011
;
;
;--------------------------------------;
;   TRAP DEFINITIONS START HERE        ;
;--------------------------------------;
;
            ;PUSH PS ON STACK
            ;R9 CONTAINS TRAP ADDRESS
            ;R8 IS USED TO HOLD THE ADDRESS OF THE PSW
            ;IF Z BIT IS SET, JUMP TO CONSOLE CODE.
            ;
            ;JUMP HERE ON ODD ADDRESS AND SSYN TIME OUT
            ;
248 BETRP:  LMI R9.K4                  ;370 TRAP TO LOC 4            /00278/   011111000 0111101 0011001 0011 000 1 11 11101101
253         SDR R8.1 STZ.CLRTT.JZF GTRP1.DBERR                       /00279/   011111101 1011111 0101000 1101 000 1 11 10110010
                                       ;R8=0, TEST AND SET Z BIT
                                       ;CLEAR TRACE TRAP F.F.
            ;
            ;JUMP HERE FOR ALL OTHER TRAPS
            ;
10  GTRAP:  ANR R8.0 STZ.CLRTT         ;12 R8=0,Z=0,CLEAR TRACE TRAP F/00285/   000001010 0001111 1001000 0001 000 1 11 10110010
250 GTRP1:  LMI R8.KL1.KM11.KNZ        ;372 R8=MAR=177776            /00286/   011111010 0000010 0011000 0011 000 0 00 00000101
42          AMA AC.GPWDI               ;412 AC=M(177776)             /00287/   000101010 0111000 0001011 0011 000 1 11 00110011
40          LMI R6.KL1.KM11.KNZ        ;400 R6=R6-2                  /00288/   000101000 0011100 0010110 0011 000 0 00 00000101
456         LMI R6.EINS.STKOV          ;401 MAR=R6                   /00289/   111001000 0011110 0010110 0011 111 1 11 11000011
488         NOP                        ;403 WAIT FOR RED ZONE STACK  /00290/   111101000 0011111 0001101 0011 000 1 11 01000011
                                       ;OVERFLOW MICRO INTERRUPT
504         NOP GWDO                   ;404 WAIT FOR TRAP            /00292/   111111000 0111101 0001101 0011 000 1 11 00011011
509         NOP PWDO                   ; M(R6)=PS                    /00293/   111111101 0110101 0001101 0011 000 1 11 01111011
            ;
            ;PUSH PC ON STACK
            ;
501         LMI R6.KL1.KM11.KNZ        ;405 R6=R6-2                  /00297/   111110101 0110000 0010110 0011 000 0 00 00000101
496         LMI R6.EINS.STKOV          ;406 MAR=R6                   /00298/   111110000 0010011 0010110 0011 111 1 11 11000011
304         NOP                        ;407 WAIT FOR RED ZONE STACK  /00299/   100110000 0110110 0001101 0011 000 1 11 01000011
                                       ;OVERFLOW MICRO INTERRUPT.
310 TSVPC:  ILR R7.GWDO                ;667 M(R6)=PC                 /00301/   100110110 0010000 0000111 0011 000 1 11 00011011
262         NOP PWDO                   ;662 WAIT FOR BUS             /00302/   100000110 0110100 0001101 0011 000 1 11 01111011
            ;
            ;PICK UP NEW PC
            ;POWER FAIL TRAP ENTERS HERE
            ;
260 PFTRP:  LMI R9.1.GWDI              ;404 MAR=R9.R9=R9+1           /00307/   100000100 0110111 0011001 1111 000 1 11 00010011
263         ADR R9.1.WDI               ;R9=R9+1                      /00308/   100000111 0111111 0111001 1111 000 1 11 01010011
271         AMA AC.PWDI                ;AC=M(MAR)                    /00309/   100001111 0001101 0001011 0011 000 1 11 01110011
223         SDR R7.1.KA1               ;R7=AC                        /00310/   011011111 0001001 0100111 1111 000 0 11 01000011
            ;
            ;PICK UP NEW PS
            ;
159         LMI R9.GWDI                ;MAR=R9                       /00314/   010011111 0111110 0011001 0011 000 1 11 00010011
158         AMA AC.PWDI                ;AC=NEW PS                    /00315/   010011110 0010010 0001011 0011 000 1 11 01110011
302         LMI R8.GWDO                ;MAR=PSW                      /00316/   100101110 0010111 0011000 0011 000 1 11 00011011
382         SDR R9.1.PWDO.JMP FETCH    ;R9=0; SET PSW                /00317/   101111110 0101011 0101001 1111 000 1 11 01111011
;
;DOUBLE BUS ERROR WHEN DOING A TRAP, OR BUS
;ERPOR WHEN IN CONSOLE MODE.
;
251 DBERR:  ANR R9                                                   /00322/   011111011 0111110 1001001 0011 000 1 11 01000011
254         LMI R9.KTPS.KL1.KTY        ;373 MAR=PUNCH STATUS REG     /00323/   011111110 0001110 0011001 0011 000 0 10 00101101
                                       ;OUTPUT A "?" AND JUMP TO
                                       ;CONSOLE.
238 OUTQM:  AMA AC.GPWDI.JFL TSTQM.QMRDY ;PUNCH READY                /00326/   011101110 1001110 0001011 0011 000 1 11 00110011
234 TSTQM:  TZR AC.KM10.K0.JMP OUTQM                                 /00327/   011101010 0111110 1011101 0011 000 1 01 11111101
235 QMRDY:  ANR AC                                                   /00328/   011101011 0110111 1001101 0011 000 1 11 01000011
231         LMI AC.KQM                 ;AC="?"                       /00329/   011100111 0111100 0011101 0011 000 1 11 00000001
236         LMI R9.KTPB.KL1.KTY        ;MAR=PUNCH                    /00330/   011101100 0111101 0011001 0011 000 0 10 00100101
237         ANR R9.GPWDO.JMP CONSL     ;OUTPUT BUFFER                /00331/   011101101 0101110 1001001 0011 000 1 11 00111011
;
;
;
;--------------------------------------;
;   INSTPUCTION DEFINITIONS START HEPE ;
;--------------------------------------;
;
;
;SPECIAL CODE TO MAKE MOV, CMP, ADD, AND SUB RR MODE GO FAST
;
84  MOVRR:  ILR R0.PG1        ;AC=S                                  /00342/   001010100 0011000 0000000 0011 000 1 10 01000011
308         NOP SMOV1.SMOV2.JMP WDESR  ;MAR=PC.SET PSW               /00343/   110000100 0000000 0001101 0011 000 1 01 00101110
;
85  CMPRR:  ILR R0.PG2.EGWDI           ;AC=D                         /00345/   001010101 0011010 0000000 0011 000 1 00 10010011
```

```
421             CIA AC           ;AC=NOT AC                          /00346/   110100101 0011100 0011111 0011 000 1 11 01000011
453             SDR T.1.KA1.SETD1.SETD2               ;T=AC          /00347/   111000101 0011101 0101100 1111 000 0 01 00000010
469             ILR R0.RG1                 ;AC=S                     /00348/   111010101 0111111 0000000 0011 000 1 10 01000011
479             NOP SETS1.SETS2                                      /00349/   111011111 0011001 0001101 0011 000 1 10 00000010
415             ILR T.1.KA1.SCMP1.SCMP2    ;AC=(NOT D)+S+1           /00350/   110011111 0111101 0001100 1111 000 0 00 10110110
413 TFFET:      NOP JMP FFET               ;PS TIME TO PROP          /00351/   110011101 0100111 0001101 0011 000 1 11 01000011
;
86  ADDRR:      ILR R0.RG1                 ;AC=S                     /00353/   001010110 0011100 0000000 0011 000 1 10 01000011
454             SDR T.1.KA1.SETS1.SETS2    ;T=AC                     /00354/   111000110 0110100 0101100 1111 000 0 10 00000010
452             ILR R0.RG2                 ;AC=D                     /00355/   111000100 0011110 0000000 0011 000 1 00 01000011
484             NOP SETD1.SETD2                                      /00356/   111100100 0110110 0001101 0011 000 1 01 00000010
486             ILR T.KA1.SADD1.SADD2.JMP WDESR ;AC=S+D              /00357/   111100110 0100100 0001100 0011 000 0 00 01101110
;
87  SUBRR:      ILR R0.RG1                 ;AC=S                     /00359/   001010111 0010111 0000000 0011 000 1 10 01000011
375             CIA AC           ;AC=NOT AC                          /00360/   101110111 0110110 0011111 0011 000 1 11 01000011
374             SDR T.1.KA1.SETS1.SETS2      ;T=AC                   /00361/   101110110 0000010 0101100 1111 000 0 10 00000010
38              ILR R0.RG2                 ;AC=D                     /00362/   000100110 0110011 0000000 0011 000 1 00 01000011
35              NOP SETD1.SETD2                                      /00363/   000100011 0000011 0001101 0011 000 1 01 00000010
51              ILR T.1.KA1.SSUB1.SSUB2.JMP WDESR ;AC=D+(NOT S)+1    /00364/   000110011 0100100 0001100 1111 000 0 00 10110110
;
48  TST:        NOP STST1.STST2.JZR FETCH   ;D=D                     /00366/   000110000 0101011 0001101 0011 000 1 01 01101110
;
50  BIT:        ANR T.KA1.EGWDI            ;T=T AND AC               /00368/   000110010 0111100 1001100 0011 000 0 11 10010011
60              ILR T.SBIT1.SBIT2.JZR FETCH ;AC=T                    /00369/   000111100 0101011 0001100 0011 000 1 01 00101110
;
104 HALT:       NOP JZR CONSL                                        /00371/   001101000 0101110 0001101 0011 000 1 11 01000011
;
105 IWAIT:      NOP EGPWT.BUSWT            ;CAUSES BUS OWNERSHIP TO WAIT  /00373/   001101001 0000010 0001101 0011 101 1 11 10100011
41              NOP JMP IWAIT              ;FOR INTERRUPT.           /00374/   000101001 0000110 0001101 0011 000 1 11 01000011
;
                ;POP PC OFF OF STACK
106 RTI:        LMI R6.1.GWDI              ;152 MAR=R6, R6=R6+1      /00377/   001101010 0000101 0010110 1111 000 1 11 00010011
90              ADR R6.1.WDI               ;432 R6=R6+1              /00378/   001011010 0111000 0110110 1111 000 1 11 01010011
88              AMA AC.PWDI                ;131 AC=M(MAR)            /00379/   001011000 0001000 0001011 0011 000 1 11 01110011
136             SDR R7.1.KA1               ;430 R7=NEW PC            /00380/   010001000 0110111 0100111 1111 000 0 11 01000011
                ;POP PS OFF OF STACK
135             LMI R6.1.GWDI              ;427 MAR=R6, R6=R6+1      /00382/   010000111 0110110 0010110 1111 000 1 11 00010011
134             ADR R6.1.WDI               ;426 R6=R6+1              /00383/   010000110 0001001 0110110 1111 000 1 11 01010011
150             AMA AC.PWDI                ;425 AC=M(MAR)            /00384/   010010110 0110111 0001011 0011 000 1 11 01110011
151             LMI R9.KL1.KM11.KN2        ;424 MAR=177776           /00385/   010010111 0111000 0011001 0011 000 0 00 00000101
152             SDR R9.1.GPWDO             ;544 R9=0, AND SET PSW    /00386/   010011000 0001010 0101001 1111 000 1 11 00111011
168             NOP SETTT.JMP FETCH        ;551 SET TRACE TRAP F.F. IF RTI/00387/   010101000 0101011 0001101 0011 000 1 11 00110010
;
107 BPT:        LMI R9.K14.JZR GTRAP       ;DO TRAP TO LOC 14        /00389/   001101011 0101010 0011001 0011 000 1 11 11001101
;
108 IOT:        LMI R9.K20.JZR GTRAP       ;DO TRAP TO LOC 20        /00391/   001101100 0101010 0011001 0011 000 1 11 10111101
;
109 RESET:      NOP EPASE.BREST.JZR FETCH  ;155 DO A RESET ON BUS    /00393/   001101101 0101011 0001101 0011 110 1 11 11100011
;
110 RTT:        NOP JMP RTI                ;LOGIC ONLY SETS TRACE TRAP F.F/00395/   001101110 0111010 0001101 0011 000 1 11 01000011
                                           ;IF RTI INSTRUCTION IN IR REG
;
102 MARK:       ILR T                      ;AC=INST                  /00398/   001100110 0010001 0001100 0011 000 1 11 01000011
278             ILR AC.KA1                 ;INST=INST*2              /00399/   100010110 0110000 0001101 0011 000 0 11 01000011
272             TZR AC.KM01.K77            ;INST=INST AND 177        /00400/   100010000 0001110 1011101 0011 000 1 10 00000001
224             ADR R6.KA1                 ;SP=SP+2*NN               /00401/   011100000 0001101 0110110 0011 000 0 11 01000011
208             ILR R5                     ;AC=R5                    /00402/   011010000 0110001 0000101 0011 000 1 11 01000011
209             SDR R7.1.KA1               ;R7=R5                    /00403/   011010001 0001110 0100111 1111 000 0 11 01000011
                ;POP OLD R5 OFF OF STACK
225             LMI R6.1.GWDI              ;MAR=R6,R6=R6+1           /00405/   011100001 0001011 0010110 1111 000 1 11 00010011
177             ADR R6.1.WDI               ;R6=R6+1                  /00406/   010110001 0111101 0110110 1111 000 1 11 01010011
189             AMA AC.PWDI                ;AC=M(MAR)                /00407/   010111101 0001001 0001011 0011 000 1 11 01110011
157             SDR R5.1.KA1.JZR FETCH     ;R5=AC                    /00408/   010011101 0101011 0100101 1111 000 0 11 01000011
;
64  INVI1:      LMI R9.K10.JZR GTRAP       ;100 INVALID INSTRUCTION  /00410/   001000000 0101010 0011001 0011 000 1 11 11011101
466  INVI2:    'LMI R9.K10.JZR GTRAP       ; TRAP TO LOC 10          /00411/   111010010 0101010 0011001 0011 000 1 11 11011101
111 INVI3:      LMI R9.K10.JZR GTRAP       ;157                      /00412/   001101111 0101010 0011001 0011 000 1 11 11011101
;
97  YESBR:      ILR T                      ;141 AC=T=INSTRUCTION     /00414/   001100001 0011010 0001100 0011 000 1 11 01000011
417             TZR T.KM11.K77             ;T=T AND 377              /00415/   110100001 0110100 1011100 0011 000 1 00 00000001
420             TZR AC.KM10.K0             ;AC=GARBAGE, AC(7)=1      /00416/   110100100 0011111 1011101 0011 000 1 01 11111101
500             SDR AC.JFL BSIG0.BSIG1     ;AC=-1                    /00417/   111110100 1001100 0101101 0011 000 1 11 01000011
450 BSIG0:      SDR AC.1                   ;702 AC=0.SIGN=0          /00418/   111000010 0110011 0101101 1111 000 1 11 01000011
451 BSIG1:      ILR T.KL1.K0               ;703 AC=SIGN EXTEND OFFSET  /00419/   111000011 0110000 0001100 0011 000 0 11 11111101
448 BRNEG:      ILR AC.KA1                 ;AC=OFFSET*2              /00420/   111000000 0110001 0001101 0011 000 0 11 01000011
449             ILR R7.KA1.JMP FETCH       ;R7=R7+OFFSET*2           /00421/   111000001 0101011 0000111 0011 000 0 11 01000011
;
96  NOBR:        NOP EGWDI.JMP FFET        ;NO BRANCH                /00423/   001100000 0100111 0001101 0011 000 1 11 10010011
;
;        EITHER SET OR CLR COND. CODES:
98  CL:         ILR T                      ;142 AC=T (INSTRUCTION)   /00426/   001100010 0011111 0001100 0011 000 1 11 01000011
498             TZR AC.K40                 ;VALID INSTR TEST         /00427/   111110010 0110011 1011101 0011 000 1 11 01111101
499             ILR T.JFL INVI2.SECL0      ;RESTORE AC=T, JUMP ILLEGAL  /00428/   111110011 1001101 0001100 0011 000 1 11 01000011
467 SECL0:      TZR AC.K17                 ;AC=AC AND 17             /00429/   111010011 0110000 1011101 0011 000 1 11 11000001
464             TZR T.K20                  ;TEST IF SET/CLR          /00430/   111010000 0011110 1011100 0011 000 1 11 10111101
480             LMI R9.KL1.KM11.KN2.JFL SECL1.SECL2                  /00431/   111100000 1001110 0011001 0011 000 0 00 00000101
                                           ;740 MAR=177776
;        CLEAR CC
```

```
482 SECL1:  CIA AC.GWDIP               ;742 AC=NOT AC              /00434/   111100010 0111001 0011111 0011 000 1 11 00010111
489         ANM AC.KA1.PWDIP.JMP SEZ   ;442 AC=AC AND PS           /00435/   111101001 0110101 1001011 0011 000 0 11 01110111
;
;       SET CC
483 SECL2:  ORM AC.KA1.GPWDP           ;743 AC=AC OR PS            /00438/   111100011 0110101 1101011 0011 000 0 11 00110111
485 SE2:    SDR R9.1.JMP WDESW         ;443 563 R9=0               /00439/   111100101 0100000 0101001 1111 000 1 11 01000011
;
100 EMT:    LMI R9.K30.JZR GTRAP       ;TRAP TO LOC 30             /00441/   001100100 0101010 0011001 0011 000 1 11 10011101
;
101 TRAP:   LMI R9.K34.JZR GTRAP       ;145 TRAP TO LOC 34         /00443/   001100101 0101010 0011001 0011 000 1 11 10001101
;
103 SOB:    ILR R0.RG1                 ;147 AC=R(N)                /00445/   001100111 0011001 0000000 0011 000 1 10 01000011
407         SDR R0.RG1.KA1             ;627 R(N)=AC-1              /00446/   110010111 0011111 0100000 0011 000 0 10 01000011
503         TZR R0.RG1.KA1             ;622 R(N) ZERO?             /00447/   111110111 0111110 1010000 0011 000 0 10 01000011
510         ILR T.JFL SOBR0.SOBR1      ;462 AC=T...JUMP FOR ZERO   /00448/   111111110 1001010 0001100 0011 000 1 11 01000011
426 SOBR0:  LMI R7.EGWDI.JMP FFET      ;503 NO.GO TO FETCH         /00449/   110101010 0100111 0010111 0011 000 1 11 10010011
427 SOBR1:  TZR AC.KM00.K77            ;502  AC=AC AND 77          /00450/   110101011 0110000 1011101 0011 000 1 11 00000001
416         CIA AC.1.JMP BRNEG         ;AC= -(AC)                  /00451/   110100000 0011100 0011111 1111 000 1 11 01000011
;
20  ROR:    SRA AC.SROR1.SROR2.JPX 0   ;DO A ROR                   /00453/   000010100 1111000 0001111 0011 000 1 11 01010110
;
21  ROL:    ILR AC.KA1.SROL1.SROL2.JPX 0 ;DO A ROL                 /00455/   000010101 1111000 0001101 0011 000 0 11 11010110
;
22  ASR:    SRA AC.SASR1.SASR2.JPX 0   ;26 DO A ASR                /00457/   000010110 1111000 0001111 0011 000 1 11 01001110
;
23  ASL:    ILR AC.KA1.SASL1.SASL2.JPX 0 ;DO A ASL                 /00459/   000010111 1111000 0001101 0011 000 0 11 11000110
;
89  RTS:    ILR R0.RG2                 ;AC=R(N)                    /00461/   001011001 0010111 0000000 0011 000 1 00 01000011
377         SDR R7.1.KA1               ;R7=AC                      /00462/   101111001 0011000 0100111 1111 000 0 11 01000011
            ;POP TOP ELEMENT OFF OF STACK
393         LMI R6.1.GWDI              ;MAR=R6.R6=R6+1             /00464/   110001001 0011010 0010110 1111 000 1 11 00010011
425         ADR R6.1.WDI               ;R6=R6+1                    /00465/   110101001 0111000 0110110 1111 000 1 11 01010011
424         AMA AC.PWDI                ;AC=M(MAR)                  /00466/   110101000 0110111 0001011 0011 000 1 11 01110011
423         SDR R0.1.KA1.RG2.JZR FETCH ;R(N)=AC                    /00467/   110100111 0101011 0100000 1111 000 0 00 01000011
;
19  SWAB:   LDI AC.1.KA1.SSWB1.SSWB2   ;AC=AC EXCHANGED            /00469/   000010011 0101000 0101111 1111 000 0 11 10111110
8           NOP SSWB3.JPX 0            ;TO FIX TIMING BUG          /00470/   000001000 1111000 0001101 0011 000 1 11 00111010
;
18  COM:    CIA AC.SCOM1.SCOM2.JPX 0   ;D=NOT D                    /00472/   000010010 1111000 0011111 0011 000 1 01 10101110
;
26  INC:    ILR AC.1.SINC1.SINC2.JPX 0 ;D=D+1                      /00474/   000011010 1111000 0001101 1111 000 1 01 00000110
;
27  DEC:    SDR AC.KA1.SDEC1.SDEC2.JPX 0 ;D=D-1                    /00476/   000011011 1111000 0101101 0011 000 0 10 00000110
;
28  NEG:    CIA AC.1.SNEG1.SNEG2.JPX 0 ;D=(NOT D)+1                /00478/   000011100 1111000 0011111 1111 000 1 00 10000110
;
16  ADC:    ILR AC.SADC1.SADC2.JPX 0   ;HARDWARE HANDLES C IN      /00480/   000010000 1111000 0001101 0011 000 1 01 01010110
;
17  SBC:    SDR AC.KA1.SSBC1.SSBC2.JPX 0 ;HARDWARE HANDLES C IN    /00482/   000010001 1111000 0101101 0011 000 0 10 10011110
;
24  BIC:    CIA T                      ;S=NOT S                    /00484/   000011000 0000011 0011110 0011 000 1 11 01000011
56          ANR T.KA1.JMP MTWD         ;T=(NOT S) AND D            /00485/   000111000 0111001 1001100 0011 000 0 11 01000011
;
25  BIS:    ORR T.KA1                  ;T=S OR D                   /00487/   000011001 0000011 1101100 0011 000 0 11 01000011
57  MTWD:   ILR T.SBCS1.SBCS2.JPX 0    ;AC=T                       /00488/   000111001 1111000 0001100 0011 000 1 01 00101110
;
30  ADD:    ILR T.KA1.SADD1.SADD2.JPX 0 ;D=D+S                     /00490/   000011110 1111000 0001100 0011 000 0 00 01101110
;
31  SUB:    SDR R8.1.KA1         ;R8=AC=D                          /00492/   000011111 0010111 0101000 1111 000 0 11 01000011
383         ILR T                      ;AC=T=S                     /00493/   101111111 0011000 0001100 0011 000 1 11 01000011
399         CIA AC                     ;S=NOT S                    /00494/   110001111 0111110 0011111 0011 000 1 11 01000011
398         NOP SETS1.SETS2                                        /00495/   110001110 0101111 0001101 0011 000 1 10 00000010
15          ILR R8.1.KA1.SSUB1.SSUB2.JPX 0                         /00496/   000001111 1111000 0001000 1111 000 0 00 10110110
;
29  XOR:    SDR T.1.KA1                ;T=AC                       /00498/   000011101 0000011 0101100 1111 000 0 11 01000011
61          ILR R0.RG1                 ;AC=R(N)                    /00499/   000111101 0111110 0000000 0011 000 1 10 01000011
62          XNR T.KA1                  ;T=T XNOR AC                /00500/   000111110 0000010 1111100 0011 000 0 11 01000011
46          ILR T                      ;AC=T                       /00501/   000101110 0111101 0001100 0011 000 1 11 01000011
45          CIA AC.SXOR1.SXOR2.JPX 0   ;55 AC=NOT AC               /00502/   000101101 1111000 0011111 0011 000 1 01 00101110
;
33  IJMP:   SDR R7.1.KA1.JZR FETCH     ;R(7)=D ADDRESS             /00504/   000100001 0101011 0100111 1111 000 0 11 01000011
;
36  JSR:    SDR T.1.KA1                ;T=D ADDRESS. T IS TMP      /00506/   000100100 0010111 0101100 1111 000 0 11 01000011
372         ILR R0.RG1                 ;AC=R(N)                    /00507/   101110100 0110101 0000000 0011 000 1 10 01000011
373         LMI R6.KN2.KL1.KM11        ;R6=R6-2                    /00508/   101110101 0111000 0010110 0011 000 0 00 00000101
376         LMI R6.EINS.STKOV          ;MAR=R(6)                   /00509/   101111000 0011000 0010110 0011 111 1 11 11000011
392         NOP                        ;WAIT FOR RED ZONE STACK    /00510/   110001000 0111100 0001101 0011 000 1 11 01000011
                                       ;OVERFLOW MICRO INTERRUPT.
396         NOP GWDO                                               /00512/   110001100 0011001 0001101 0011 000 1 11 00011011
412         NOP PWDO                   ;NEED TO WAIT FOR BUS       /00513/   110011100 0011010 0001101 0011 000 1 11 01111011
428         LMI T                      ;MAR=NEXT PC                /00514/   110101100 0111110 0011100 0011 000 1 11 01000011
430         ILR R7.EGWDI               ;AC=R7                      /00515/   110101110 0111111 0000111 0011 000 1 11 10010011
431         SDR R0.1.KA1.RG1           ;R(N)=R7                    /00516/   110101111 0011011 0100000 1111 000 0 10 01000011
447         ILR T                      ;AC=T(TMP)                  /00517/   110111111 0111110 0001100 0011 000 1 11 01000011
446         SDR R7.1.KA1.JMP FFET      ;R7=TMP                     /00518/   110111110 0100111 0100111 1111 000 0 11 01000011
;
34  CLR:    TZR AC.SCLR1.SCLR2.JPX 0   ;42 D=0                     /00520/   000100010 1111000 1011101 0011 000 1 01 01101110
;
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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The CMU-11 is a microprogrammable processor built with the Intel 3000 microcomputer set that emulates the PDP-11 architecture. In addition, it has been designed to provide full Unibus support. The enclosed documentation gives the details of the CMU-11 design. This documentation has been generated in conjuction with the Stanford Drawing System, the SAGE simulator, and the Intel 3000 microassembler. Those hoping to do any further development of the CMU-11 design are encouraged to also use these design aids and all of the CMU-11 design information shown here (and other information such as ROM contents and wirelists) are available on magnetic tape. See the following report for an introductory discussion and evaluation of the

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20. ABSTRACT (continued)

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McWilliams, T. M., S. H. Fuller, and W. H. Sherwood, "Using LSI Provessor Bit-Slice to Build a PDP-11: A Case Study in Microcomputer Design," Technical Report, Department of Computer Science, Carnegie-Mellon University, Pittsburgh, PA, 15213.